



STIC EIC 2100 103513

Search Request Form 34

Today's Date:

9/10/03

What date would you like to use to limit the search?

Priority Date: 10/13/00

Other:

Name Chongshan Chen

AU 2172 Examiner # 79547

Room # 4B25 Phone 305-8319

Serial # 09/687,453

Format for Search Results (Circle One):

PAPER

DISK

EMAIL

Where have you searched so far?

USP

DWPI

EPO

JPO

ACM

IBM TDB

IEEE

INSPEC

SPI

Other

Is this a "Fast & Focused" Search Request? (Circle One) YES NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at <http://ptoweb/patents/stic/stic-tc2100.htm>.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

A graphics system, comprising a plurality of graphics processing units; and a memory controller connected between ~~the~~ graphics memory access bus and graphics processing units, said memory controller providing a non-partitioned view of said graphics memory to said plurality of graphics processing units, while dividing said graphics memory access bus into individual bus partitions, each of which is fraction of the graphics memory access bus size, said memory controller partitioning information within said graphics memory into ~~it~~ independently accessible memory partitions said memory controller routing data from said independently accessible memory partitions to said plurality of graphics processing unit via said individual bus partitions.

STIC Searcher

Geoffrey St Leger

Phone

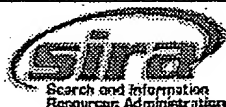
308-7800

Date picked up

9/10/03

Date Completed

9/10/03





STIC Search Report

EIC 2100

STIC Database Tracking Number: 103513

TO: Chongshan Chen
Location: 4B25
Art Unit : 2172
Wednesday, September 10, 2003

Case Serial Number: 09/687453

From: Geoffrey St. Leger
Location: EIC 2100
PK2-4B30
Phone: 308-7800

geoffrey.stleger@uspto.gov

Search Notes

Dear Examiner Chen,

Attached please find the results of your Fast & Focus search request for application 09/687453. I searched Dialog's foreign patent files and technical databases.

Please let me know if you have any questions.

Regards,

Geoffrey St. Leger
4B30/308-7800



STIC Search Results Feedback Form

EIC 2100

Questions about the scope or the results of the search? Contact *the EIC searcher* or contact:

Anne Hendrickson, EIC 2100 Team Leader
308-7831, CPK2-4B40

Voluntary Results Feedback Form

➤ I am an examiner in Workgroup: Example: 3730

➤ Relevant prior art **found**, search results used as follows:

- ☐ 102 rejection
- ☐ 103 rejection
- ☐ Cited as being of interest.
- ☐ Helped examiner better understand the invention.
- ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
(journal articles, conference proceedings, new product announcements etc.)

➤ Relevant prior art **not found**:

- ☐ Results verified the lack of relevant prior art (helped determine patentability).
- ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2100 CPK2-4B40



8/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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06425294 **Image available**
MEMORY CONTROLLER

PUB. NO.: 2000-010857 [JP 2000010857 A]
PUBLISHED: January 14, 2000 (20000114)
INVENTOR(s): HIRABAYASHI MASAYUKI
TAKEUCHI TOSHIFUMI
APPLICANT(s): HITACHI LTD
APPL. NO.: 10-178221 [JP 98178221]
FILED: June 25, 1998 (19980625)
INTL CLASS: G06F-012/04; G06F-013/16

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **memory controller** in which the data bus width of a memory is not fixed.

SOLUTION: This controller has a data selector 3 which switches input data buses having different bus widths and data selector 4 which **divides** the output data **buses** of the memory in one-byte or multi-byte units and selects and outputs desired data from the **divided** data **buses**. A memory control circuit 1 controls them to input and output data to and from the data buses having the different bus widths.

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8/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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05866211 **Image available**
MEMORY CONTROLLER

PUB. NO.: 10-149311 [JP 10149311 A]
PUBLISHED: June 02, 1998 (19980602)
INVENTOR(s): MARUYAMA TERUYUKI
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-323387 [JP 96323387]
FILED: November 20, 1996 (19961120)
INTL CLASS: [6] G06F-012/00; G11C-011/406
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent the reduction of the memory access speed by deciding the urgency of memory control based on the number of stored memory access requests and the number of pending refresh operations.

SOLUTION: A bus I/F selector 102 receives the memory access requests from a **bus** 101 to **divide** them into the requests S1a and S1b at each preference level of requests and queues them into the request queues 103a and 103b. An arbitration circuit 105 receives a refresh request S2 from a refresh circuit 104 and the requests S1a and S1b from the queues 103a and 103b respectively and arbitrates these requests. A reply data production part 108 produces the reply data based on the data S6 obtained from a memory device 107 and the request information S7 and queues the reply data into a replay queue 109. A bus-I/F 110 fetches the replay data and gives a reply to a processor.

8/5/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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05597652 **Image available**
BUS CONTROLLER

PUB. NO.: 09-212452 [JP 9212452 A]
PUBLISHED: August 15, 1997 (19970815)
INVENTOR(s): AZEZAKI TSUTOMU
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 08-015732 [JP 9615732]
FILED: January 31, 1996 (19960131)
INTL CLASS: [6] G06F-013/36; G06F-013/36; G06F-013/42
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PROBLEM TO BE SOLVED: To improve the bus use rate of a computer system which has a **split bus** .

SOLUTION: In the period wherein a **memory controller** (MMC-1) 22 holds the right to use a data bus DATA, an address control circuit 221 monitors an address request issued on an address bus ADDR and when the issue of an address request, requiring data transfer through the data bus DATA by another device, by a CPU, etc., detected, the right to use the data bus DATA is released for the 1st time. Consequently, the **memory controller** (MMC-1) 22 which has obtained the data bus right once need not release the bus unless an address request like this is issued, so the data bus can be used continuously until another device requires the data bus. Therefore, the frequency of arbitration can be decreased and the bus use rate of the computer system having the **split bus** can be improved.

8/5/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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04665939 **Image available**
CPU DEVICE

PUB. NO.: 06-337839 [JP 6337839 A]
PUBLISHED: December 06, 1994 (19941206)
INVENTOR(s): KAWASHIMA HIDEYUKI
 TSUJIOKA SHIGEO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 05-128697 [JP 93128697]
FILED: May 31, 1993 (19930531)
INTL CLASS: [5] G06F-013/18
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PURPOSE: To efficiently use a memory by providing a bus idle field showing whether memory access is to be executed in an instruction code.

CONSTITUTION: An instruction when CPU 101 executes is **divided** into the **bus** idle field 301 and an instruction field 302. How many instructions that CPU 101 does not use a memory exist or how long clock does in continue is stored in the bus idle field 301 by a compiler or a programmer in the flow of a program. The bus idle field 301 is stored in a bus idle register in CPU 101 and the value is reported to a **memory controller** 102 by an external signal. The **memory controller** 102 judges a bus idle state from CPU 101 and processes a memory transfer request whose priority is low from an I/O device 104 only when transfer can be terminated within the idle time.

8/5/7 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO
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04151748 **Image available**

MEMORY CONTROLLER

PUB. NO.: 05-143448 [JP 5143448 A]
PUBLISHED: June 11, 1993 (19930611)
INVENTOR(s): SASAKI SHINICHI
 AIHARA HIDETOSHI
APPLICANT(s): YOKOGAWA ELECTRIC CORP [000650] (A Japanese Company or
 Corporation), JP (Japan)
APPL. NO.: 03-303325 [JP 91303325]
FILED: November 19, 1991 (19911119)
INTL CLASS: [5] G06F-012/06; G06F-012/08; G06F-012/08
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1619, Vol. 17, No. 532, Pg. 5,
 September 24, 1993 (19930924)

ABSTRACT

PURPOSE: To improve the efficiency of access to a memory by distributing the memory for the unit of a cache line.

CONSTITUTION: Assuming that processors 10-14 generate cache error at the same time and respectively requests access to cache line unit memories #0-#3, first of all, the processor 10 generates a read request cycle to a memory bank 100. Because of **split** read, a **bus** line 500 is opened while the memory side interprets and processes the read request. During this operation, the processor 20 generates a read request cycle to a memory bank 200. Similarly, the processor 30 generates a read request cycle to a memory bank 300 before a read response cycle from the memory bank 200, and the processor 40 generates a read request cycle to a memory bank 400 before a read response cycle from the memory bank 300. Thus, the possibility of access competition is reduced.

8/5/8 (Item 8 from file: 347)

DIALOG(R)File 347:JAPIO

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03800338 **Image available**

MEMORY ACCESS SYSTEM

PUB. NO.: 04-165438 [JP 4165438 A]
PUBLISHED: June 11, 1992 (19920611)
INVENTOR(s): MURATA TORU
APPLICANT(s): NEC ENG LTD [329822] (A Japanese Company or Corporation), JP
 (Japan)
APPL. NO.: 02-291640 [JP 90291640]
FILED: October 29, 1990 (19901029)
INTL CLASS: [5] G06F-012/02; G06F-013/28; G06F-015/64
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.4
 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 1428, Vol. 16, No. 463, Pg. 37,
 September 25, 1992 (19920925)

ABSTRACT

PURPOSE: To speed up access to a large-capacity memory by performing direct memory access (DMA) transfer by up to four bytes at each time by using a main bus and a subordinate bus simultaneously.

CONSTITUTION: When a memory 4 for image processing is accessed fast, a main bus controller 2 and a subordinate bus controller 3 are put in fast access mode with a signal for mode control and serve as **memory controllers** 2A and 3A. Further, the 16-bit data lines of the main **bus** and subordinate **bus** are **divided** into bands 1 - 4 of high-order eight bits and low-order eight bits and the DMA transfer of every four bits can be performed at the same time. The **memory controllers** 2A and 3A are associated with each other to generate a write and a read signal for image data to 16-Mbyte memories 4A - 4D. Consequently, the fast access mode wherein the two multi buses are used is entered, so large-amount image data is written and read fast.

8/5/9 (Item 9 from file: 347)
DIALOG(R) File 347:JAPIO
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02222037 **Image available**
MICROPROCESSOR DEBUGGING DEVICE

PUB. NO.: 62-138937 [JP 62138937 A]
PUBLISHED: June 22, 1987 (19870622)
INVENTOR(s): ISHIDA TOSHIHIRO
APPLICANT(s): YOKOGAWA ELECTRIC CORP [000650] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-279446 [JP 85279446]
FILED: December 12, 1985 (19851212)
INTL CLASS: [4] G06F-011/28
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)
JOURNAL: Section: P, Section No. 641, Vol. 11, No. 366, Pg. 67, November 28, 1987 (19871128)

ABSTRACT

PURPOSE: To obtain a microprocessor debugging device capable of **bus** tracing and **breaking** on a physical address basis by fetching addresses converted by a **memory controller**.

CONSTITUTION: A probe 2a can mount a **memory controller** 12 detached from a target board 1 and the 1st multiplexer 13 which selects a logical address outputted by a microprocessor 11 or the address of the base part of a physical address outputted by the memory control part 12 and the 2nd multiplexer 14 which selects the address of the extended part of the physical address outputted by the **memory controller** or zero data are arranged, so that the logical address or physical address is obtained from the composite output of the 1st and the 2nd multiplexers optionally. Thus, selections are made by the multiplexers to extract the logical address or physical address optionally, and this is sent to a main device side and utilized for tracing an address bus.

8/5/10 (Item 10 from file: 347)
DIALOG(R) File 347:JAPIO
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01976545 **Image available**
MEMORY CONTROLLER

PUB. NO.: 61-190645 [JP 61190645 A]
PUBLISHED: August 25, 1986 (19860825)
INVENTOR(s): ONO MASAHIRO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-030745 [JP 8530745]
FILED: February 19, 1985 (19850219)
INTL CLASS: [4] G06F-012/16; G06F-011/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 536, Vol. 11, No. 15, Pg. 113, January 16, 1987 (19870116)

ABSTRACT

PURPOSE: To facilitate the access by providing registers corresponding to n- number of equally divided areas of a memory and storing a value larger than n-1 in registers corresponding to areas having defective positions and holding values increases successively by one in the other registers.

CONSTITUTION: A **memory controller** 100 connected to a common bus 4 and

an address signal line 5 consists of a memory 2, an address comparing circuit 6, and a memory test circuit 7, and the memory 2 is divided equally into n- number of areas, and registers whose number of bits is larger than $\log(\text{sub } 2)n$ are provided in the circuit 6 correspondingly to individual areas. When the upper digit of the address common to individual divided areas and stored data of registers coincide with each other, **divided** areas are connected to the **bus 4**, and write and read data in individual addresses of the memory 2 are compared with each other by the circuit 7; and if they do not coincide with each other, a value larger than n-1 is held in the register corresponding to the area including the address of disaccord between write and read data, and values increased successively by one are held in the other registers.

8/5/13 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

013746625 **Image available**
WPI Acc No: 2001-230854/200124
XRPX Acc No: N01-164588

Information processor e.g. multiprocessor type PC has bus memory controller which divides processor buses and PCI buses into specific groups, so that each group operates independently and mutually

Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001034571	A	20010209	JP 99202836	A	19990716	200124 B

Priority Applications (No Type Date): JP 99202836 A 19990716

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 2001034571 A 11 G06F-013/14

Abstract (Basic): JP 2001034571 A

NOVELTY - The bus **memory controller** (210) equipped with physical **divide** function, **divides** several processor **buses** (102,112) and PCI buses (131-134) into specific groups (201,202), such that each group operates independently and mutually.

USE - E.g. multiprocessor type personal computer.

ADVANTAGE - By **dividing buses** into several groups, personal computer of single multiprocessor component is obtained and hence failure resistant equivalent to multiplexing by several PC, is materialized, thereby offering cost reduction.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of PC.

Processor buses (102,112)
PCI buses (131-134)
Bus groups (201,202)
Bus **memory controller** (210)
pp; 11 DwgNo 1/8

Title Terms: INFORMATION; PROCESSOR; MULTIPROCESSOR; TYPE; BUS; MEMORY;
CONTROL; DIVIDE; PROCESSOR; BUS; BUS; SPECIFIC; GROUP; SO; GROUP; OPERATE
; INDEPENDENT; MUTUAL

Derwent Class: T01

International Patent Class (Main): G06F-013/14

International Patent Class (Additional): G06F-011/20; G06F-015/173

File Segment: EPI

8/5/14 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012909677 **Image available**
WPI Acc No: 2000-081513/200007
XRPX Acc No: N00-064776

Memory device for computer - has several memory groups divided into pairs of memory modules of identical capacity based on connection position of memory controller with bus wiring

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11330394	A	19991130	JP 98136323	A	19980519	200007 B

Priority Applications (No Type Date): JP 98136323 A 19980519

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11330394	A	8	H01L-027/10	

Abstract (Basic): JP 11330394 A

NOVELTY - Several memory groups are divided into memory module pairs of identical capacity. The division is determined by connection position of **memory controller** (203) to bus wiring (121,101).

USE - In electronic computer.

ADVANTAGE - Enables HF operation with low data propagation time.

DESCRIPTION OF DRAWING(S) - The figure shows the memory device **divided** into two modules. (121,101) **Bus** Wirings; (203) **Memory controller**

Dwg.1/12

Title Terms: MEMORY; DEVICE; COMPUTER; MEMORY; GROUP; DIVIDE; PAIR; MEMORY; MODULE; IDENTICAL; CAPACITY; BASED; CONNECT; POSITION; MEMORY; CONTROL; BUS; WIRE

Derwent Class: T01; U14

International Patent Class (Main): H01L-027/10

File Segment: EPI

8/5/15 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012597815 **Image available**

WPI Acc No: 1999-403921/199934

XRPX Acc No: N99-301001

Latency monitoring apparatus for pending transaction in computer system bus structure

Patent Assignee: NCR CORP (NATC)

Inventor: MCDONALD E A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5919268	A	19990706	US 97925982	A	19970909	199934 B

Priority Applications (No Type Date): US 97925982 A 19970909

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5919268	A	10	G06F-011/00	

Abstract (Basic): US 5919268 A

NOVELTY - A divider logic receives TOTAL QUALIFIED CYCLES count value from one counter (501) and TOTAL LATENCY CLOCKS value from another counter (511) to divide TOTAL QUALIFIED CYCLES count value by TOTAL LATENCY CLOCK value to determine average number of clocks of latency per bus cycle, during receipt of selective signals.

DETAILED DESCRIPTION - The counter (501) connected to Intel Pentium Pro (P6) bus, contains TOTAL QUALIFIED CYCLES count value which is incremented on the start of every bus cycle during receipt of qualified increment signal. The counter (511) is incremented on every clock cycle occurring during sample period by number of outstanding bus cycle to provide TOTAL LATENCY CLOCKS count value. An INDEPENDENT CLAIM is also included for latency monitoring method of pending transaction in computer system.

USE - For monitoring latency of pending transaction within

symmetric multiprocessor in computer system **bus** structures supporting pipelining or **split** transactions.

ADVANTAGE - Reduces number of hardware for monitoring latency characteristic by qualifying bus cycle. The counter is large enough to support counting, by maximum number of pending qualified **bus** transactions. Allows the **divider** logic to be built into any ASIC at minimal cost and allows performance monitoring of latency characteristic.

DESCRIPTION OF DRAWING(S) - The figure represents block diagram illustrating divider logic within advanced **memory controller**.

Counters (501,511)

pp; 10 DwgNo 5A,5B/5

Title Terms: LATENT; MONITOR; APPARATUS; PENDING; TRANSACTION; COMPUTER; SYSTEM; BUS; STRUCTURE

Derwent Class: T01

International Patent Class (Main): G06F-011/00

File Segment: EPI

8/5/16 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012088937 **Image available**

WPI Acc No: 1998-505848/199843

XRPX Acc No: N98-394306

Signal integrating apparatus for PCB of computer system - has resistor group provided for each transmission line of bus, which comprises series of resistors divided into two portions of first and second segments, respectively

Patent Assignee: APPLE COMPUTER INC (APPY)

Inventor: BUUCK D C; DHUEY M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5805030	A	19980908	US 95511349	A	19950804	199843 B

Priority Applications (No Type Date): US 95511349 A 19950804

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5805030	A	8	H01P-003/00	

Abstract (Basic): US 5805030 A

The apparatus includes a bus (80) consisting of multiple transmission lines (81-88) each of which having a resistor groove (90) of series of resistors (91-98). The resistors of each transmission line are divided into two portions (100,110) comprising first and second segments of low resistance respectively.

The resistor group has resistance value approximately equal to the impedance value of the corresponding transmission line. A processor (10) and a cache memory (20) are electrically connected to the portion (100). Also a **memory controller** (40) and a PCI controller (30) are connected to the portion (110).

ADVANTAGE - Reduces crosstalk and creates local isolation for devices connected on bus.

Dwg. 4/5

Title Terms: SIGNAL; INTEGRATE; APPARATUS; PCB; COMPUTER; SYSTEM; RESISTOR; GROUP; TRANSMISSION; LINE; BUS; COMPRISE; SERIES; RESISTOR; DIVIDE; TWO; PORTION; FIRST; SECOND; SEGMENT; RESPECTIVE

Derwent Class: T01; W02

International Patent Class (Main): H01P-003/00

File Segment: EPI

8/5/17 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011915919 **Image available**

WPI Acc No: 1998-332829/199829

XRPX Acc No: N98-259847

Memory control arrangement for computer system - has multiplexer through which simultaneous accesses of main memory by CPU and peripheral device is performed with help of respect buses

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)

Inventor: WU W; YANG G

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5761727	A	19980602	US 96626363	A	19960402	199829 B

Priority Applications (No Type Date): US 96626363 A 19960402

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5761727	A	6	G06F-012/00	

Abstract (Basic): US 5761727 A

The arrangement divides a main memory (240) into main memory segment (260) and shared resource segment (270). The peripheral devices and CPU (110) are connected to the respective segments of the main memory. The data stored in the CPU is transferred to main segment whereas the data from CPU and peripheral device are transferred to the shared resource segment. The data is transferred from CPU, peripheral device to the shared resource segment is done through a shared data path (250). The shared data path includes two independent data paths, respectively connecting CPU to main memory segment. The peripheral device and CPU are simultaneously connected to resource segment to send data path according to necessity.

A main **memory controller** (220) selectively connects peripheral device to shared resource segment. The multiplexer is cooperatively operated with shared data path, according to the connection state. The main **memory controller** is connected to two access control **buses** for controlling the **divided** main memory. The simultaneous access of main memory by CPU and peripheral device is carried by independent bus through the multiplexer.

ADVANTAGE - Enhances system efficiency and throughput.

Dwg.2/2

Title Terms: MEMORY; CONTROL; ARRANGE; COMPUTER; SYSTEM; MULTIPLEX; THROUGH ; SIMULTANEOUS; ACCESS; MAIN; MEMORY; CPU; PERIPHERAL; DEVICE; PERFORMANCE; HELP; RESPECT; BUS

Derwent Class: T01

International Patent Class (Main): G06F-012/00

File Segment: EPI

8/5/18 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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011546909 **Image available**

WPI Acc No: 1997-523390/199748

XRPX Acc No: N97-436053

Sharing type external storage device for computer - has external memory controller which controls access to memory medium in predetermined order

Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 9251351	A	19970922	JP 9659688	A	19960315	199748 B

Priority Applications (No Type Date): JP 9659688 A 19960315

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 9251351	A	8	G06F-003/06	

Abstract (Basic): JP 9251351 A

The device consists of a disk apparatus (12) which is accessed by a number of computers (11). The commands published by the computers are controlled by an external **memory controller** (13).

The external **memory controller** controls access of the disk apparatus in an order of reception of commands. The commands are output to the disk apparatus through an output unit.

ADVANTAGE - Guarantees maximum throughput value. Provides uniform execution time. Offers reliability. Increases efficiency. Increases speed of operation. Facilitates communication even when communication **bus** between control apparatus **breaks** down.

Dwg.1/5

Title Terms: SHARE; TYPE; EXTERNAL; STORAGE; DEVICE; COMPUTER; EXTERNAL; MEMORY; CONTROL; CONTROL; ACCESS; MEMORY; MEDIUM; PREDETERMINED; ORDER
Derwent Class: T01; T03; W04
International Patent Class (Main): G06F-003/06
International Patent Class (Additional): G11B-019/02
File Segment: EPI

8/5/19 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010816637 **Image available**

WPI Acc No: 1996-313590/199632

XRFX Acc No: N96-263757

Data-processing system for increasing loading capacity of memory - has automatic memory controller that access data processor to memory device during abnormal operation of other local bus

Patent Assignee: FUJITSU LTD (FUJIT)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8137709	A	19960531	JP 94280683	A	19941115	199632 B

Priority Applications (No Type Date): JP 94280683 A 19941115

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 8137709	A	24	G06F-011/20	

Abstract (Basic): JP 8137709 A

The system (1) has a data processor (2) which is connected to an automatic **memory controller** (4) through a local bus. The automatic **memory controller** sequentially provides memory access to a data processor.

ADVANTAGE - Provides continuous data processing by using **memory controller** which is used when other local **bus** **breaks** down.

Dwg.2/21

Title Terms: DATA; PROCESS; SYSTEM; INCREASE; LOAD; CAPACITY; MEMORY; AUTOMATIC; MEMORY; CONTROL; ACCESS; DATA; PROCESSOR; MEMORY; DEVICE; ABNORMAL; OPERATE; LOCAL; BUS
Derwent Class: T01
International Patent Class (Main): G06F-011/20
International Patent Class (Additional): G06F-013/00; G06F-015/16
File Segment: EPI

8/5/20 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010048778 **Image available**

WPI Acc No: 1994-316489/199439

XRFX Acc No: N94-248598

Computer system incorporating memory controller - operates using burst operations and with ISA and EISA bus masters and has state machine provided for use with cache controller and state machine provided for use

with EISA and ISA bus masters

Patent Assignee: COMPAQ COMPUTER CORP (COPQ)

Inventor: HAMID M A; THOME G W

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5353423	A	19941004	US 91719030	A	19910621	199439 B

Priority Applications (No Type Date): US 91719030 A 19910621

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5353423	A	44	G06F-012/00	

Abstract (Basic): US 5353423 A

The computer system includes a system bus including address, data and control **bus portions** and a processor. A write-back cache system connected to the processor and coupled to the system bus controls operations on the system bus. The write-back cache system includes a cache controller and data memories. A number of memory devices are coupled to the system bus. A **memory controller** coupled to the system bus and the memory devices controls operation of the memory devices.

An external bus includes address, data and control **bus portions**. An external bus interface and controller coupled to the system bus and the external bus converts system bus operations to external bus operations and external bus operations to system bus operations. An external bus master coupled to the external bus controls operations on the external bus, some of which may be directed to the memory devices on the system bus.

ADVANTAGE - **Memory controller** handles all simultaneous functions to allow max. computer system performance.

Dwg.1/22

Title Terms: COMPUTER; SYSTEM; INCORPORATE; MEMORY; CONTROL; OPERATE; BURST ; OPERATE; ISA; BUS; MASTER; STATE; MACHINE; CACHE; CONTROL; STATE; MACHINE; ISA; BUS; MASTER

Derwent Class: T01

International Patent Class (Main): G06F-012/00

File Segment: EPI

8/5/21 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010028242 **Image available**

WPI Acc No: 1994-295955/199437

XRPX Acc No: N94-232834

Computer system with pipelining and concurrent controller for memory - has memory controller formed of number of simple state machines interlinked but operating separately with knowledge of speed of memory blocks

Patent Assignee: COMPAQ COMPUTER CORP (COPQ)

Inventor: BONELLA R M; COLLINS M J; LANDRY J A; SANTELER P A; THOME G W

Number of Countries: 015 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 617365	A1	19940928	EP 94302014	A	19940322	199437 B
CA 2119174	A	19940923	CA 2119174	A	19940316	199444
US 5537555	A	19960716	US 9334290	A	19930322	199634
CA 2119174	C	19981020	CA 2119174	A	19940316	199901
EP 617365	B1	20010613	EP 94302014	A	19940322	200134
DE 69427421	E	20010719	DE 627421	A	19940322	200148
			EP 94302014	A	19940322	

Priority Applications (No Type Date): US 9334290 A 19930322

Cited Patents: EP 339224; EP 440457; EP 465847

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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EP 617365 A1 E 86 G06F-013/16
 Designated States (Regional): AT BE CH DE DK ES FR GB IE IT LI NL SE
 CA 2119174 A G06F-012/02
 US 5537555 A 89 G06F-013/00
 CA 2119174 C G06F-012/02
 EP 617365 B1 E G06F-013/16
 Designated States (Regional): AT BE CH DE DK ES FR GB IE IT LI NL SE
 DE 69427421 E G06F-013/16 Based on patent EP 617365

Abstract (Basic): EP 617365 A

The computer system includes a processor board, system board and I/O interface board. The system board provides interfaces to different buses. The processor board has a Pentium computer (152) with address (PA), data (PD) and control (PC) buses feeding the rest of the system. Memory operations are controlled by a **memory controller** (156).

The **memory controller** consists of a number of simple state machines each controlling one aspect of memory operations. These interact with each other and have knowledge of memory block speed to allow different access control for each memory block.

ADVANTAGE - Allows for pipelining and concurrent operations while using only simple state machines.

Dwg.4/69

Title Terms: COMPUTER; SYSTEM; PIPE; CONCURRENT; CONTROL; MEMORY; MEMORY; CONTROL; FORMING; NUMBER; SIMPLE; STATE; MACHINE; INTERLINKED; OPERATE; SEPARATE; SPEED; MEMORY; BLOCK

Derwent Class: T01

International Patent Class (Main): G06F-012/02; G06F-013/00; G06F-013/16

File Segment: EPI

8/5/22 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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009786056 **Image available**

WPI Acc No: 1994-065909/199408

Related WPI Acc No: 1993-154228; 1996-159850; 1998-239634; 1998-609472

XRPX Acc No: N94-051553

Fault tolerant wafer scale integrated circuit system - uses high speed interface to control transfer of large amounts of data between functional modules and bus master

Patent Assignee: MONOLITHIC SYSTEM TECHNOLOGY (MONO-N); HSU F (HSUF-I);

LEUNG W Y (LEUN-I); MONOLITHIC SYSTEM TECHNOLOGY INC (MONO-N)

Inventor: HSU F; LEUNG W Y; LEUNG W

Number of Countries: 021 Number of Patents: 013

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9403901	A1	19940217	WO 93US7262	A	19930805	199408	B
AU 9347987	A	19940303	AU 9347987	A	19930805	199426	
EP 654168	A1	19950524	EP 93918585	A	19930805	199525	
			WO 93US7262	A	19930805		
JP 8500687	W	19960123	WO 93US7262	A	19930805	199642	
			JP 94505501	A	19930805		
US 5592632	A	19970107	US 91787984	A	19911105	199708	
			US 92865410	A	19920408		
			US 92927564	A	19920810		
			US 94307496	A	19940914		
			US 95469887	A	19950606		
US 5613077	A	19970318	US 91787984	A	19911105	199717	
			US 92865410	A	19920408		
			US 92927564	A	19920810		
			US 94307496	A	19940914		
US 5666480	A	19970909	US 91787984	A	19911105	199742	
			US 92865410	A	19920408		
			US 92927564	A	19920810		
			US 94307496	A	19940914		
			US 95484063	A	19950606		
EP 654168	B1	20011031	EP 93918585	A	19930805	200169	

			WO 93US7262	A	19930805	
US 20010039601	A1	20011108	US 91787984	A	19911105	200171
			US 92865410	A	19920408	
			US 92927564	A	19920810	
			US 94307496	A	19940914	
			US 95484063	A	19950606	
			US 97820297	A	19970318	
			US 2001903094	A	20010710	
DE 69331061	E	20011206	DE 631061	A	19930805	200203
			EP 93918585	A	19930805	
			WO 93US7262	A	19930805	
US 6425046	B1	20020723	US 91787984	A	19911105	200254
			US 92865410	A	19920408	
			US 92927564	A	19920810	
			US 94307496	A	19940914	
			US 95484063	A	19950606	
			US 97820297	A	19970318	
			US 97820297	A	19970318	
US 6483755	B2	20021119	US 91787984	A	19911105	200280
			US 92865410	A	19920408	
			US 92927564	A	19920810	
			US 94307496	A	19940914	
			US 95484063	A	19950606	
			US 97820297	A	19970318	
			US 2001903094	A	20010710	
US 20030051091	A1	20030313	US 91787984	A	19911105	200321
			US 92865410	A	19920408	
			US 92927564	A	19920810	
			US 94307496	A	19940914	
			US 95484063	A	19950606	
			US 97820297	A	19970318	
			US 2001903094	A	20010710	
			US 2002273442	A	20021015	

Priority Applications (No Type Date): US 92927564 A 19920810; US 91787984 A 19911105; US 92865410 A 19920408; US 94307496 A 19940914; US 95469887 A 19950606; US 95484063 A 19950606; US 97820297 A 19970318; US 2001903094 A 20010710; US 2002273442 A 20021015

Cited Patents: US 3585378; US 3651473; US 3761879; US 4092733; US 4227045; US 4319356; US 4605928; US 4615017; US 4627058; US 4639861; US 4648298; US 4653050; US 4663758; US 4667328; US 4719621; US 4872137; US 4881232; US 4926382; US 4943966; US 4955020; US 4970724; US 4984192; US 4985895; US 5077737; US 5077738; US 5103424; US 5111434; US 5133064; US 5159273; US 5187779; US 5218686

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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WO 9403901	A1	E	76	G11C-029/00	
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Designated States (National): AU CA JP KR

Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

AU 9347987	A			G11C-029/00	Based on patent WO 9403901
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EP 654168	A1	E	54	G11C-029/00	Based on patent WO 9403901
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Designated States (Regional): DE FR GB

JP 8500687	W		96	G06F-013/00	Based on patent WO 9403901
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US 5592632	A		30	G06F-011/20	CIP of application US 91787984
					CIP of application US 92865410
					Cont of application US 92927564
					Div ex application US 94307496
US 5613077	A		32	G06F-013/00	CIP of application US 91787984
					CIP of application US 92865410
					Cont of application US 92927564
US 5666480	A		30	G06F-011/34	CIP of application US 91787984
					CIP of application US 92865410
					Cont of application US 92927564
					Div ex application US 94307496
					Div ex patent US 5613077

EP 654168	B1	E		G06F-011/20	Based on patent WO 9403901
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Designated States (Regional): DE FR GB

US 20010039601	A1	G06F-013/00	CIP of application US 91787984 CIP of application US 92865410 Cont of application US 92927564 Div ex application US 94307496 Div ex application US 95484063 Cont of application US 97820297 Div ex patent US 5613077 Div ex patent US 5666480
DE 69331061	E	G06F-011/20	Based on patent EP 654168 Based on patent WO 9403901
US 6425046	B1	G11C-007/00	CIP of application US 91787984 CIP of application US 92865410 Cont of application US 92927564 Div ex application US 94307496 Div ex application US 95484063 CIP of application US 97820297 Div ex patent US 5613077 Div ex patent US 5666580
US 6483755	B2	G06F-012/08	CIP of application US 91787984 CIP of application US 92865410 Cont of application US 92927564 Div ex application US 94307496 Div ex application US 95484063 Cont of application US 97820297 Div ex patent US 5613077 Div ex patent US 5666480
US 20030051091	A1	G06F-012/00	CIP of application US 91787984 CIP of application US 92865410 Cont of application US 92927564 Div ex application US 94307496 Div ex application US 95484063 Cont of application US 97820297 Cont of application US 2001903094 Div ex patent US 5613077 Div ex patent US 5666480 Cont of patent US 6425046 Cont of patent US 6483755

Abstract (Basic): WO 9403901 A

The fault tolerant IC system includes a low speed tester (1407) connected only to the system bus interface (1405) of the **memory controller** (1403), with the operating frequency set at a speed suitable for the tester without compromising the hierarchical bus (1402). All the high speed signals are shielded from the tester.

In operation, the **memory controller** serves as a bridge between the memory modules and the CPU and Direct Memory Access controller. Synchronisation between the receiving unit of the memory interface (1404) and the sending unit of the system interface uses memory in which the input port is controlled by the receiving clock but the output port is controlled by the system clock.

ADVANTAGE - Provides system with performance that is not affected by defects in bus or modules. Permits programmable reconfiguration to bus network.

Dwg.14/30

Title Terms: FAULT; TOLERATE; WAFER; SCALE; INTEGRATE; CIRCUIT; SYSTEM; HIGH; SPEED; INTERFACE; CONTROL; TRANSFER; AMOUNT; DATA; FUNCTION; MODULE; BUS; MASTER

Derwent Class: T01; U13

International Patent Class (Main): G06F-011/20; G06F-011/34; G06F-012/00; G06F-012/08; G06F-013/00; G11C-007/00; G11C-029/00

International Patent Class (Additional): G01R-031/02; G06F-001/12; G06F-011/10; G06F-011/16; G06F-012/06; G06F-012/16; G06F-013/40; G11C-008/00; G11C-013/00; H04L-025/02

File Segment: EPI

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008271001

WPI Acc No: 1990-158002/199021

XRPX Acc No: N90-122789

Multiple posting cache memory - uses multiple posting facilities to allow higher level of processor utilisation when dealing with external devices

Patent Assignee: COMPUADD CORP (COMP-N)

Inventor: BATTERSHEL B; GRIFFITH J

Number of Countries: 013 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 369935	A	19900523	EP 89730185	A	19890811	199021 B

Priority Applications (No Type Date): US 88270249 A 19881114

Cited Patents: 1.Jnl.Ref; A3...9142; EP 149392; NoSR.Pub

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 369935	A			

Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE

Abstract (Basic): EP 369935 A

The computer comprises a central processing unit (10) which outputs control, data, and address signals required to write required to write to a memory location; a bus connecting the processor to the memory via a **memory controller** (22) and bus posting logic circuits (23) associated with the **memory controller**. The computer has an internal bus (12) for coprocessor and cache, and separate memory and device **buses splitting** from the internal **bus**.

Multiple posting circuits (34) improve the speed at which the CPU writes to various locations. One posting circuit (23) is associated with the **memory controller** (22) and another posting circuit (25) is associated with the bus controller (24). Multiple devices (28-32) are connected to the bus controller over a device bus (26). A cache memory (28) increases the speed of reads from a predetermined range of memory addresses.

USE/ADVANTAGE - Computer with improved posting facilities to reduce wait state count needed to match the processor to slower devices. (6pp Dwg.No.1/2

Title Terms: MULTIPLE; POST; CACHE; MEMORY; MULTIPLE; POST; FACILITY; ALLOW ; HIGH; LEVEL; PROCESSOR; UTILISE; DEAL; EXTERNAL; DEVICE

Derwent Class: T01

International Patent Class (Additional): G06F-012/08

File Segment: EPI

8/5/24 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007258924

WPI Acc No: 1987-255931/198736

XRPX Acc No: N87-191355

TV video signals processing set - with additional memory connected to access controller by input

Patent Assignee: SOYUZGIPROVODKHOZ (SOYU-R)

Inventor: BERNSHTEIN M N; MINSKII D E; POLYAKOV M E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
SU 1285623	A	19870123	SU 3936921	A	19850731	198736 B

Priority Applications (No Type Date): SU 3936921 A 19850731

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
SU 1285623	A	7		

Abstract (Basic): SU 1285623 A

Shorter time of processing video signals is achieved with the direct addressing of the video store by the processor. The unit includes an auxiliary memory, with input connected to the access controller, while the group of leads is linked to the group of processor leads by bidirectional bus. Furthermore, it is connected to A-D converter, to video processor and to a third group of leads of video **memory controller**. The input of the latter is tied to the other output of the access controller while the output of the video processor feeds the input of the video monitor.

The zone of the memory addressed by the processor (1) when using the system **bus** is **divided** into two parts: one part of constantly addressable memory zone, and a page-addressable zone. During the addressing of the first part, the data exchange cycle involves the main memory block (2), while addressing the other part involves a cycle of data exchange with the additional maskable memory (4) or with the video memory (7) when the controller (6) is implicated. The latter features three interfaces for the system bus, for the bus exchanging video information with the video processor (8) or with the A-D converter (10). Conflicting conditions are prevented by programming the converter through the bus for receiving analog TV signal from the source (11).

USE/ADVANTAGE - Means of processing and displaying data using computer technology e.g. in medicine and scientific research. The unit ensures checking of programme implementation with its monitor-indicating changes of the data on the stack of the computer without slowing down of programme characteristics. Bul.3/23.1.87.

Dwg.1/4

Title Terms: TELEVISION; VIDEO; SIGNAL; PROCESS; SET; ADD; MEMORY; CONNECT; ACCESS; CONTROL; INPUT

Derwent Class: T01; W04

International Patent Class (Additional): H04N-005/66

File Segment: EPI

12/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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06317819 **Image available**
BUS ACCESS SYSTEM AND BUS ACCESS CONTROLLER

PUB. NO.: 11-259417 [JP 11259417 A]
PUBLISHED: September 24, 1999 (19990924)
INVENTOR(s): SAKASHITA YOHEI
APPLICANT(s): FUJITSU LTD
APPL. NO.: 10-063062 [JP 9863062]
FILED: March 13, 1998 (19980313)
INTL CLASS: G06F-013/36; G06F-013/16

ABSTRACT

PROBLEM TO BE SOLVED: To provide a bus access system with an improved bus availability constituted of a data bus and an address bus to execute simultaneous read/write accesses by dividing bus width into a plurality of sub-buses.

SOLUTION: A **controller** is provided with a **bus** division part 110 for **dividing** a data **bus** of a prescribed bit width into a plurality of sub-buses having arbitrary bus width, and a bus control part 120 which independently controls access of the sub-buses divided by the bus division part 110, and simultaneously reads/ writes data against the device of an access object in a sub-bus unit.

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12/5/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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06124446 **Image available**
ADDRESS SPACE ALLOCATING SYSTEM

PUB. NO.: 11-065983 [JP 11065983 A]
PUBLISHED: March 09, 1999 (19990309)
INVENTOR(s): HIRAI TOMONORI
SATO SHINICHI
KAMIYAMA YOHEI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 09-231048 [JP 97231048]
FILED: August 27, 1997 (19970827)
INTL CLASS: G06F-013/14

ABSTRACT

PROBLEM TO BE SOLVED: To efficiently allocate the use address space of each interface card to the address space of an I/O bus controller.

SOLUTION: The use address space of each interface card 22 is allocated to the address space of an I/O bus controller 21 applied from a CPU 2 in a computer system connecting an I/O bus 6, to which plural interface cards 22 are connected, through the I/O bus controller 21 to the CPU 2. Concerning such an address space allocating system, the address space of the I/O **bus controller** 21 is **divided** into the prescribed number of unit address spaces more than the number of installed interface cards 22, and the use address space of each interface card 22 is allocated to the unit address spaces corresponding to the size of this use address space.

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12/5/7 (Item 7 from file: 347)
DIALOG(R) File 347:JAPIO
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05780509 **Image available**
DIRECT MEMORY ACCESS ARBITRATION SYSTEM

PUB. NO.: 10-063609 [JP 10063609 A]
PUBLISHED: March 06, 1998 (19980306)
INVENTOR(s): IKUMICHI YUICHI
APPLICANT(s): MEIDENSHA CORP [000610] (A Japanese Company or Corporation),
JP (Japan)
APPL. NO.: 08-213958 [JP 96213958]
FILED: August 14, 1996 (19960814)
INTL CLASS: [6] G06F-013/28
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a direct memory access(DMA) system excellent in the efficiency of operation.

SOLUTION: The DMA system is provided with a hold arbitration circuit 9, an accessing arbitration circuit 11 and a hold stop generating circuit 10 and allows a CPU 1 to access a part of memories even in the execution of DMA. Even in an access to the CPU 1, a DMA controller 4 can access a part of the memories. The system is also provided with a register 12 to monitor an access state and to easily execute control. Since memories included in the same systems as **controllers** (CPU and DMA **controllers**) **divided** through a local **bus** buffer 6 can be optionally accessed, the CPU 1 can access a part of the memories even in the DMA and the controller 4 can access a part of the memories even in the period of an access to the CPU 1, so that the system can be more quickly constructed.

12/5/8 (Item 8 from file: 347)
DIALOG(R) File 347:JAPIO
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05265857 **Image available**
COMPUTER SYSTEM PROVIDED WITH PLURAL BUSES, BUS CONNECTION DEVICE AND BUS CONTROL METHOD

PUB. NO.: 08-221357 [JP 8221357 A]
PUBLISHED: August 30, 1996 (19960830)
INVENTOR(s): MOCHIDA TETSUYA
KOBAYASHI ICHII
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 07-023148 [JP 9523148]
FILED: February 10, 1995 (19950210)
INTL CLASS: [6] G06F-013/362; G06F-013/36
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PURPOSE: To construct a computer system for connecting non-split buses in multiple stages by receiving access requests from respective plural bus devices and mediating a bus access right.

CONSTITUTION: An inter-bus controller (bus connection controller) 115 is provided so as to mediate the entire access of the non- **split buses**. The inter- **bus controller** 115 receives bus request informing signals and read lock signals and performs mediation so as not to parallelly generate plural read accesses on the non-split buses in the entire system. Thus, when the plural non-split buses are present and the access requests are simultaneously generated, only the access request to one bus is permitted and the mediation is performed so as not to simultaneously perform access

in the plural non-split buses. Since the other access request is not permitted while the access for the access request is executed, hung-up is avoided and the non-split buses are connected in the multiple stages.

12/5/9 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
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05140399 **Image available**
DMA TRANSFER CONTROLLER

PUB. NO.: 08-095899 [JP 8095899 A]
PUBLISHED: April 12, 1996 (19960412)
INVENTOR(s): INAI HIDENORI
AIMOTO TAKESHI
IWAMOTO HIROSHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 06-227587 [JP 94227587]
FILED: September 22, 1994 (19940922)
INTL CLASS: [6] G06F-013/28
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers &
Microprocessors)

ABSTRACT

PURPOSE: To provide an I/O device, which is connected to a high-performance split type I/O bus, with a high-throughput, low-latency DMA transfer control function.

CONSTITUTION: On the I/O device, plural controllers 123 and 124 which serve bus requests outputted to a split bus at the same time, a buffer 112 which temporarily holds response packets to a read request, a request packet generating circuit 111 which generates request packets from the outputs of the controllers 123 and 124, and a response packet processing circuit 110 which distributes the services of the response packets to corresponding read controllers are provided, and, by constituting the controllers 123 and 124 dividing into a function which services request packets and a function which services response packets, parallel processing in the controllers is made possible. Since not only the parallel operation of the controllers which serves a bus transaction, but also the parallel operation in the controllers are made possible, the DMA transfer controller which has higher performance than before is obtained.

12/5/10 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO
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04868025 **Image available**
DATA TRANSFER DEVICE

PUB. NO.: 07-160625 [JP 7160625 A]
PUBLISHED: June 23, 1995 (19950623)
INVENTOR(s): UNOSAWA SUSUMU
OTA KAZUKO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company
or Corporation), JP (Japan)
APPL. NO.: 05-309107 [JP 93309107]
FILED: December 09, 1993 (19931209)
INTL CLASS: [6] G06F-013/28
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)

ABSTRACT

PURPOSE: To attain the fast data communication by generating and transmitting at one time the memory addresses of both the transferring side and the transfer destination when the data are transferred to a memory from

another.

CONSTITUTION: A data transfer device is provided with a DMA controller 1, a CPU 2, the memories 3 and 4, an address converter part 5 which converts the address received from the controller 1, and a buffer control part 6 which divides the bus set between the controller 1 and the CPU 2. When a DMA request signal 7 is supplied to the controller 1, the controller 1 outputs an HLDRQ signal 8 to the part 6. Then the part 6 outputs an HLDK signal 9 to the controller 1. Furthermore the address sent from the controller 1 is converted at the part 5, and the addresses of both memories 3 and 4 are generated and transmitted at a time.

12/5/11 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

03970357 **Image available**
BUS ARBITRATION SYSTEM

PUB. NO.: 04-335457 [JP 4335457 A]
PUBLISHED: November 24, 1992 (19921124)
INVENTOR(s): NUMATA HIROYUKI
APPLICANT(s): YOKOGAWA ELECTRIC CORP [000650] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-105915 [JP 91105915]
FILED: May 10, 1991 (19910510)
INTL CLASS: [5] G06F-013/26; G06F-013/36
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1518, Vol. 17, No. 182, Pg. 105, April 08, 1993 (19930408)

ABSTRACT

PURPOSE: To constitute the system so that a bus controller connected to a shared memory holds fairness of priority between bus controllers to which a processor is connected in a split bus by fixing the priority of the bus acquisition right in the system to the highest level, and also, to improve the bus acquisition rate of the shared memory and the bus controller in which an access is concentrated.

CONSTITUTION: In a multi-processor system of a single bus coupling type, processors 10(sub 1)-10(sub n-1) and a shared memory 10(sub n) are connected to a split bus 30 through bus controllers 20(sub 1)-20(sub n). As for the bus controllers 20(sub 1)--20(sub n) there are those which have processor interfaces 21(sub 1)-21(sub n-1) being interfaces to the processors 10(sub 1)-10(sub n-1), and that which has a memory interface 21(sub n) being an interface to the shared memory 10(sub n). In such a state, as for each bus controller 20(sub 1)-20(sub n-1) connected to the processors 10(sub 1)-10(sub n-1), respectively, the bus acquisition priority is determined, based on a round robin system.

12/5/12 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2003 JPO & JAPIO. All rts. reserv.

03733340 **Image available**
BUS DIAGNOSTIC DEVICE

PUB. NO.: 04-098440 [JP 4098440 A]
PUBLISHED: March 31, 1992 (19920331)
INVENTOR(s): YOSHIOKA ATSUSHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-212643 [JP 90212643]
FILED: August 10, 1990 (19900810)
INTL CLASS: [5] G06F-013/00; G06F-011/00
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.1

JOURNAL: Section: P, Section No. 1389, Vol. 16, No. 333, Pg. 23, July
20, 1992 (19920720)

ABSTRACT

PURPOSE: To reduce a hardware required for diagnosing a **bus** by vertically **dividing** a **bus** . which connects a **controller** and a device to be controll, into two buses, defining them as an input bus and an output bus respectively, and transmitting/receiving data.

CONSTITUTION: When setting a bus diagnostic mode, a control signal is transmit ted from a device 2 to be controlled to a three state gate 10, and the direction of the three state gate is decided. For example, a BUS 1 is defined as the output bus and a BUS 2 is defined as the input bus. Then, a test data outputted from the device 2 to be controlled passes the route of BUS 2-> three state gate 10-> BUS 2 and comes back to the device 2 to be controlled again. At the device 2 to be controlled, the output data is compared with the input data for each bit, and the normality of the bus is diagnosed. Thus, the hardware required for diagnosing the bus can be reduced, and the bus can be efficiently tested

12/5/36 (Item 19 from file: 350)
DIALOG(R) File 350: Derwent WPIX
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010958684 **Image available**
WPI Acc No: 1996-455634/199645
XRPX Acc No: N96-383884

Bus structure for multiprocessor system - has logical buses each formed of physical buses, and connected to memory unit via physical memory bus and to bus switching unit

Patent Assignee: INT BUSINESS MACHINES CORP (IBM)
Inventor: GETZLAFF K; LEPPLA B; TAST H; WILLE U; GETZLAFF K J
Number of Countries: 018 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9630842	A1	19961003	WO 95EP1140	A	19950327	199645 B
EP 760979	A1	19970312	EP 95913163	A	19950327	199715
			WO 95EP1140	A	19950327	
JP 9506731	W	19970630	WO 95EP1140	A	19950327	199736
			JP 96528822	A	19950327	
US 5889969	A	19990330	WO 95EP1140	A	19950327	199920
			US 96737951	A	19961127	
JP 3086261	B2	20000911	WO 95EP1140	A	19950327	200046
			JP 96528822	A	19950327	

Priority Applications (No Type Date): WO 95EP1140 A 19950327

Cited Patents: EP 141332; US 4807184; US 5337411

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9630842	A1	E	32	G06F-013/40	
				Designated States (National):	JP US
				Designated States (Regional):	AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
EP 760979	A1	E		G06F-013/40	Based on patent WO 9630842
				Designated States (Regional):	DE FR GB
JP 9506731	W		33	G06F-003/00	Based on patent WO 9630842
US 5889969	A			G06F-013/00	Based on patent WO 9630842
JP 3086261	B2		15	G06F-003/00	Previous Publ. patent JP 9506731
					Based on patent WO 9630842

Abstract (Basic): WO 9630842 A

The bus structure is used for a multiprocessor system consisting of processors (1,2,3,4) with a main memory formed by two memory banks each comprising of two memory modules (5,6,7,8), which are controlled by storage **controllers** (9,10). The common **bus** is **divided** into two logical **buses** (11,12). Each of the logical buses includes a bus switching unit (BSU) (13,14), and each of the processors (1,2,3,4) is connected to each of the BSUs (13,14), to form a bus network with four physical buses (0L,0R,1L,1R).

The BSUs (13,14) connect the four physical buses on the processor side to the memory banks (5,6,7,8) via memory buses (15,16). The number of logical buses (11,12) equals the number of BSUs (13,14). The BSUs (13,14) contain bus arbitration functions for controlling access to the logical buses (11,12).

USE - Multiple bus structure for multiprocessor systems with multiple level cache, for handling near end signal reception problems, if more processors are interconnected via bus system.

ADVANTAGE - Provides high degree of system modularity w.r.t extension and reduction of computer system. Maximises point-to-point connectivity between bus participants.

Dwg.1/11

Title Terms: BUS; STRUCTURE; MULTIPROCESSOR; SYSTEM; LOGIC; BUS; FORMING; PHYSICAL; BUS; CONNECT; MEMORY; UNIT; PHYSICAL; MEMORY; BUS; BUS; SWITCH; UNIT

Derwent Class: T01

International Patent Class (Main): G06F-003/00; G06F-013/00; G06F-013/40

International Patent Class (Additional): G06F-012/08; G06F-013/16;

G06F-015/16

File Segment: EPI

12/5/37 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010655912 **Image available**
WPI Acc No: 1996-152865/199616
XRPX Acc No: N96-128399

**Computer system supporting several bus configurations - stores
dynamically time slot assignment value responsive to central processing
unit used to dynamically divide access time to one bus controller
among other controller**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)

Inventor: LEUNG W L

Number of Countries: 005 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 702307	A1	19960320	EP 95305223	A	19950726	199616 B
JP 8063429	A	19960308	JP 95168644	A	19950704	199620
US 5598542	A	19970128	US 94287213	A	19940808	199710
JP 3231583	B2	20011126	JP 95168644	A	19950704	200201

Priority Applications (No Type Date): US 94287213 A 19940808

Cited Patents: EP 28891; EP 519350; US 5297292

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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EP 702307	A1	E	23 G06F-013/40	
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Designated States (Regional): DE FR GB

JP 8063429	A	23 G06F-013/36
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US 5598542	A	22 G06F-013/372
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JP 3231583	B2	23 G06F-013/362	Previous Publ. patent JP 8063429
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Abstract (Basic): EP 702307 A

The computer system includes a central processing unit (CPU, 50) with a host processor bus (52). Several bus controller (70 and 80) communicate with the CPU to control the transfer of information over the buses. A centralised bus arbiter (90) arbitrates accesses between each of the peripheral buses.

A dynamically alterable time slot assignment register communicates with the CPU and the bus arbiter to dynamically store a time slot assignment value responsive to the CPU. The value is used to dynamically divide the access time to one of the bus controllers among the other controllers.

USE/ADVANTAGE - Relates to computer system architecture and multibus dynamic arbiter. Allows dynamic and more equitable allocation of memory bus bandwidth between various buses, and allocation of memory bus bandwidth between PCI bus and MCA bus.

Dwg.1/11

Title Terms: COMPUTER; SYSTEM; SUPPORT; BUS; CONFIGURATION; STORAGE;
DYNAMIC; TIME; SLOT; ASSIGN; VALUE; RESPOND; CENTRAL; PROCESS; UNIT;
DYNAMIC; DIVIDE; ACCESS; TIME; ONE; BUS; CONTROL; CONTROL

Derwent Class: T01

International Patent Class (Main): G06F-013/36; G06F-013/362; G06F-013/372;
G06F-013/40

International Patent Class (Additional): G06F-013/16

File Segment: EPI

12/5/38 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010231569 **Image available**
WPI Acc No: 1995-132826/199518
Related WPI Acc No: 1996-289109; 1996-289120
XRPX Acc No: N95-104509

Single-chip microcomputer for home game console or portable data

communications terminal - has divided internal bus with break controller for selectively connecting first and second buses and third bus of lower speed connected with peripheral modules

Patent Assignee: HITACHI LTD (HITA); HITACHI MICROCOMPUTER SYSTEM (HITA-N); HITACHI MICON SYSTEM KK (HITA-N); AKAO Y (AKAO-I); HASEGAWA A (HASE-I); HAYAKAWA A (HAYA-I); ITO Y (ITOY-I); KAWASAKI S (KAWA-I); KURAKAZU K (KURA-I); MATSUBARA K (MATS-I); NOGUCHI K (NOGU-I); OHSUGA H (OHSU-I); HITACHI ULSI ENG CORP (HISC)

Inventor: AKAO Y; HASEGAWA A; HAYAKAWA A; ITO Y; KAWASAKI S; KURAKAZU K; MATSUBARA K; NOGUCHI K; OHSUGA H

Number of Countries: 006 Number of Patents: 010

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 646873	A2	19950405	EP 94112520	A	19940810	199518 B
EP 646873	A3	19950920	EP 94112520	A	19940810	199615
US 5930523	A	19990727	US 94306100	A	19940914	199936
			US 9855099	A	19980403	
US 6212620	B1	20010403	US 94306100	A	19940914	200120
			US 9855099	A	19980403	
			US 98191313	A	19981113	
US 6223265	B1	20010424	US 94306100	A	19940914	200125
			US 9855099	A	19980403	
			US 98192093	A	19981113	
US 6279063	B1	20010821	US 9855099	A	19980403	200150
			US 99467087	A	19991210	
US 20020007430	A1	20020117	US 99467087	A	19991210	200212
			US 2001918625	A	20010730	
US 20030046514	A1	20030306	US 94306100	A	19940914	200320
			US 9855099	A	19980403	
			US 98191313	A	19981113	
			US 99467087	A	19991210	
			US 2001918625	A	20010730	
			US 2002172290	A	20020613	
KR 349787	B	20030205	KR 9423490	A	19940916	200340
US 6591294	B2	20030708	US 94306100	A	19940914	200353
			US 9855099	A	19980403	
			US 99467087	A	19991210	
			US 2001918625	A	20010730	

Priority Applications (No Type Date): JP 9436472 A 19940209; JP 93255099 A 19930917

Cited Patents: No-SR.Pub; 3.Jnl.Ref; EP 346917; EP 506594; EP 523764; EP 588607; EP 624844; US 4984195

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 646873	A2	E	81	G06F-013/40	
					Designated States (Regional): DE FR GB IT
EP 646873	A3			G06F-013/40	
US 5930523	A			G06F-015/76	Cont of application US 94306100
US 6212620	B1			G06F-015/00	Cont of application US 94306100
					Cont of application US 9855099
US 6223265	B1			G06F-012/00	Cont of application US 94306100
					Cont of application US 9855099
US 6279063	B1			G06F-013/00	Div ex application US 9855099
					Div ex patent US 5930523
US 20020007430	A1			G06F-013/38	Cont of application US 99467087
US 20030046514	A1			G06F-015/00	Cont of application US 94306100
					Cont of application US 9855099
					Cont of application US 98191313
					Cont of application US 99467087
					Cont of application US 2001918625
					Cont of patent US 5930523
					Cont of patent US 6212620
					Cont of patent US 6279063
KR 349787	B			G06F-009/00	Previous Publ. patent KR 95009422
US 6591294	B2			G06F-015/16	Cont of application US 94306100
					Div ex application US 9855099
					Cont of application US 99467087

Abstract (Basic): EP 646873 A

The single chip microcomputer includes a first bus having a central processing unit connected with a cache memory, and a second bus having a dynamic memory access control circuit connected with an external bus interface. A **break controller** is connected with the first and second buses for transmitting an address signal of the first bus selectively to the second bus. A third bus is connected with a peripheral module, and has a lower bus-cycle than the first or second buses.

A bus state controller is coupled between the second and third bus for effecting a signal transfer and synchronisation between the second and third bus. A fixed point multiply and accumulate arithmetic unit is connected with the first bus, and a fixed point type divider circuit is connected with the second bus. The peripheral module includes at least one of a free running timer, a serial communication interface and a watch-dog timer.

USE/ADVANTAGE - High speed three-dimensional image processing.
Enlarges operation margin and enables access of synchronous dynamic RAM.

Dwg.1/42

Title Terms: SINGLE; CHIP; MICROCOMPUTER; HOME; GAME; CONSOLE; PORTABLE;
DATA; COMMUNICATE; TERMINAL; DIVIDE; INTERNAL; BUS; BREAK; CONTROL;
SELECT; CONNECT; FIRST; SECOND; BUS; THIRD; BUS; LOWER; SPEED; CONNECT;
PERIPHERAL; MODULE

Derwent Class: T01; W04

International Patent Class (Main): G06F-009/00; G06F-012/00; G06F-013/00;
G06F-013/38; G06F-013/40; G06F-015/00; G06F-015/16; G06F-015/76

International Patent Class (Additional): G06F-015/78

File Segment: EPI

12/5/39 (Item 22 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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010138065 **Image available**

WPI Acc No: 1995-039316/199506

XRPX Acc No: N95-031162

Cellular radio system with base stations which are capable of frequency hopping - has time divided serial bus connected between base stations transporting traffic data from station controller

Patent Assignee: MOTOROLA INC (MOTI)

Inventor: GOLDING P; HOBBS K; GOLDING P A

Number of Countries: 006 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2280087	A	19950118	GB 9313851	A	19930705	199506	B
DE 4423582	A1	19950112	DE 4423582	A	19940705	199507	
FI 9403217	A	19950106	FI 943217	A	19940705	199513	
SE 9402345	A	19950106	SE 942345	A	19940704	199513	
CA 2126947	A	19950106	CA 2126947	A	19940628	199514	
JP 7154851	A	19950616	JP 94174914	A	19940705	199533	
GB 2280087	B	19971210	GB 9313851	A	19930705	199801	

Priority Applications (No Type Date): GB 9313851 A 19930705

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2280087	A		16	H04Q-007/30	
DE 4423582	A1		8	H04B-007/26	
JP 7154851	A		8	H04Q-007/36	
FI 9403217	A			H04B-007/26	
SE 9402345	A			H04B-007/26	
CA 2126947	A			H04B-007/26	
GB 2280087	B			H04Q-007/30	

Abstract (Basic): GB 2280087 A

The base stations (20,21,22) of a cellular communications system has a serial interface (40) for direct connection over a time **divided** serial **bus** (23) to a base station **controller** (30). The traffic data is received (31) from the base station controller via the serial interface. A channel coder (31) codes the traffic data and selectively outputs it onto the serial bus for retrieval by another base station.

Preferably, the serial interfaces are arranged to receive channel coded traffic data from the serial bus. The interface also has a transmitter (24'') for transmitting that data as a radio signal.

USE/ADVANTAGE - GSM base station transceiver systems. Small cabinet required. Allows base stations to hop as group, even though only connected by CEPT-link.

Dwg.2/4

Title Terms: CELLULAR; RADIO; SYSTEM; BASE; STATION; CAPABLE; FREQUENCY; HOP; TIME; DIVIDE; SERIAL; BUS; CONNECT; BASE; STATION; TRANSPORT; TRAFFIC; DATA; STATION; CONTROL

Derwent Class: W01; W02

International Patent Class (Main): H04B-007/26; H04Q-007/30; H04Q-007/36

International Patent Class (Additional): H04B-001/713; H04B-007/12; H04Q-007/22; H04Q-007/24; H04Q-007/26

File Segment: EPI

9/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01574751

Method and apparatus for providing address parity checking for multiple overlapping address spaces on a shared bus
Verfahren und Vorrichtung zur Adressenparitätsprüfung für mehrfache überlappende Adressbereiche auf einem gemeinsamen Bus
Procédé et dispositif pour la vérification de la parité d'adresse pour des régions d'adresse multiples sur un bus partagé

PATENT ASSIGNEE:

INTEL CORPORATION, (322933), 2200 Mission College Boulevard, Santa Clara, CA 95052, (US), (Applicant designated States: all)

INVENTOR:

McWilliams, Peter D., 20145 S.W. Nancy Lane, Aloha, Oregon 97007, (US)
Pawlowski, Stephen S., 6624 S.W. 158th Avenue, Beaverton, Oregon 97007, (US)

LEGAL REPRESENTATIVE:

Molyneaux, Martyn William (34017), Wildman, Harrold, Allen & Dixon 11th Floor, Tower 3, Clements Inn,, London WC2A 2AZ, (GB)

PATENT (CC, No, Kind, Date): EP 1306766 A1 030502 (Basic)

APPLICATION (CC, No, Date): EP 2003000814 970701;

PRIORITY (CC, No, Date): US 705684 960828

DESIGNATED STATES: DE; GB; IT

RELATED PARENT NUMBER(S) - PN (AN):

EP 979454 (EP 97931545)

INTERNATIONAL PATENT CLASS: G06F-013/42; G06F-011/10; G06F-012/06

ABSTRACT WORD COUNT: 73

NOTE:

Figure number on first page: 7

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200318	400
SPEC A	(English)	200318	6278
Total word count - document A			6678
Total word count - document B			0
Total word count - documents A + B			6678

...SPECIFICATION latter case. The data phase occurs only if a transaction requires a data transfer. The data phase can be response initiated (for example, by the **memory controller** or another processor) or request initiated.

The **bus** accommodates deferred transactions by **splitting** a **bus** transaction into two independent transactions. The first transaction involves a request by a requesting agent and a response by the responding agent. In one embodiment...

9/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01417842

Bus sampling on one edge of a clock signal and driving on another edge
Bus, der auf einer Flanke eines Taktsignals abtastet und auf der anderen Flanke treibt
Echantillonnage de bus sur un front d'un signal d'horloge et pilotage sur un autre front

PATENT ASSIGNEE:

Broadcom Corporation, (2064671), 16215 Alton Parkway, Irvine, California 92618, (US), (Applicant designated States: all)

INVENTOR:

Rowlands, Joseph B., 620 Park View Drive No. 206, Santa Clara, California 95054, (US)

Cho, James Y., 924 Cherrystone Drive, Los Gatos, California 95032, (US)

LEGAL REPRESENTATIVE:

Jehle, Volker Armin, Dipl.-Ing. et al (95141), Patentanwalte Bosch, Graf von Stosch, Jehle, Fluggenstrasse 13, 80639 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1197872 A2 020417 (Basic)
APPLICATION (CC, No, Date): EP 2001308532 011005;
PRIORITY (CC, No, Date): US 680523 001006
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06F-013/42
ABSTRACT WORD COUNT: 201
NOTE:

Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200216	909
SPEC A	(English)	200216	6206
Total word count - document A			7115
Total word count - document B			0
Total word count - documents A + B			7115

...SPECIFICATION to I/O interfaces 22A-22B, and I/O bridge 20B is coupled to I/O interfaces 22C-22D. L2 cache 14 is coupled to **memory controller** 16, which is further coupled to a memory 26.

Bus 24 may be a **split transaction bus** in the illustrated embodiment. A **split transaction bus** **splits** the address and data portions of each transaction and allows the address portion (referred to as the address phase) and the data portion (referred to...

9/3,K/9 (Item 9 from file: 348)

DIALOG(R) File 348:EUROPEAN PATENTS
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01409142

Out of order associative queue in two clock domains
Nichtsequentielle assoziative Warteschlange in zwei Taktbereichen
File d'attente associative hors-sequence dans deux domaines d'horloge
PATENT ASSIGNEE:

Broadcom Corporation, (2064671), 16215 Alton Parkway, Irvine, California 92618, (US), (Applicant designated States: all)

INVENTOR:

Cho, James Y, 924 Cherrystone Drive, Los Gatos, California 95032, (US)

LEGAL REPRESENTATIVE:

Jehle, Volker Armin, Dipl.-Ing. et al (95141), Patentanwalte Bosch, Graf von Stosch, Jehle, Fluggenstrasse 13, 80639 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 1191452 A2 020327 (Basic)
APPLICATION (CC, No, Date): EP 2001308010 010920;
PRIORITY (CC, No, Date): US 665982 000920
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: G06F-013/16
ABSTRACT WORD COUNT: 192
NOTE:

Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200213	2124
SPEC A	(English)	200213	8709
Total word count - document A			10833
Total word count - document B			0
Total word count - documents A + B			10833

...SPECIFICATION hit in L2 cache 14, in which case L2 cache 14 may be the responding agent. Other embodiments may not include L2 cache 14 and **memory controller** 16 may be the responding agent for all memory transactions.

Bus 24 may be a **split transaction bus** in the illustrated embodiment. A **split transaction bus** **splits** the address and data portions of each transaction and allows the address portion (referred to as the address phase) and the data portion (referred to...

9/3,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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01234045

SYSTEM AND ADAPTER CARD FOR REMOTE CONSOLE EMULATION
SYSTEM UND ADAPTERKARTE FUR EMULATION EINER ENTFERNTEN KONSOLE
SYSTEME ET CARTE ADAPTATEUR POUR EMULATION DE CONSOLES A DISTANCE
PATENT ASSIGNEE:

UNISYS CORPORATION, (842794), Township Line and Union Meeting Roads P.O.
Box 500, Blue Bell, PA 19424-0001, (US), (Proprietor designated states:
all)

INVENTOR:

POWDERLY, Terrence, V., 10 Crown Lane, East Fallowfield, PA 19320, (US)

LEGAL REPRESENTATIVE:

Modiano, Guido, Dr.-Ing. et al (40786), Modiano, Josif, Pisanty & Staub,
Baaderstrasse 3, 80469 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 1190329 A1 020327 (Basic)
EP 1190329 B1 030312
WO 2000070472 001123

APPLICATION (CC, No, Date): EP 2000928862 000505; WO 2000US12308 000505

PRIORITY (CC, No, Date): US 310542 990512

DESIGNATED STATES (Pub A): AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE;
IT; LI; LU; MC; NL; PT; SE; (Pub B): CH; DE; GB; LI

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G06F-013/10

NOTE:

No A-document published by EPO

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200311	920
CLAIMS B	(German)	200311	847
CLAIMS B	(French)	200311	990
SPEC B	(English)	200311	7952
Total word count - document A			0
Total word count - document B			10709
Total word count - documents A + B			10709

...SPECIFICATION that the processor 26 executes is stored, and an associated local random-access memory 40, both of which interface to the processor 26 via local **bus segment** 28b. A **memory controller** 36, such as a Direct Memory Access controller (DMA), may also be interfaced to the bus segment 28b to control memory transfers to and from...

9/3,K/12 (Item 12 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

01175751

METHOD AND APPARATUS FOR HIGH SPEED DATA CAPTURE USING BIT-TO-BIT TIMING CORRECTION, AND MEMORY DEVICE USING SAME
VERFAHREN UND ANORDNUNG FUR HOCHGESCHWINDIGKEITSDATENERFASSUNG MIT KORREKTUR DER BIT-ZU-BIT-ZEITGEBUNG UND SPEICHERANORDNUNG UNTER VERWENDUNG DERSELBEN
PROCEDE ET APPAREIL DE CAPTURE RAPIDE DE DONNEES UTILISANT UNE CORRECTION DE SYNCHRONISATION BIT A BIT ET DISPOSITIF A MEMOIRE LES UTILISANT

PATENT ASSIGNEE:

MICRON TECHNOLOGY, INC., (1177691), 8000 South Federal Way, Boise, Idaho
83716-9632, (US), (Proprietor designated states: all)

INVENTOR:

KEETH, Brent, 5077 N. Fifeshire Place, Boise, ID 83713, (US)

LEGAL REPRESENTATIVE:

Hirsch, Peter, Dipl.-Ing. (44461), Klunker Schmitt-Nilson Hirsch
Winzererstrasse 106, 80797 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 1137996 A1 011004 (Basic)

EP 1137996 B1 030409

WO 2000033200 000608

APPLICATION (CC, No, Date): EP 99962858 991124; WO 99US27877 991124

PRIORITY (CC, No, Date): US 201519 981130

DESIGNATED STATES (Pub A): AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE;

IT; LI; LU; MC; NL; PT; SE; (Pub B): DE; GB; IT

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G06F-013/16

NOTE:

No A-document published by EPO

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
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CLAIMS B	(English)	200315	2225
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CLAIMS B	(German)	200315	1964
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CLAIMS B	(French)	200315	2530
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SPEC B	(English)	200315	19919
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Total word count - document A	0
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Total word count - document B	26638
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Total word count - documents A + B	26638
------------------------------------	-------

...SPECIFICATION system memory bus 23 by sending the memory devices 16a-16c command packets that contain both control and address information. Data are coupled between the **memory controller** 18 and the memory devices 16a-16c through a data **bus portion** of the system memory bus 23. During a read operation, data is transferred from the packetized memory devices 16a-16c over the memory bus 23...

9/3,K/13 (Item 13 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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01041406

METHOD AND APPARATUS FOR ADJUSTING THE TIMING OF SIGNALS OVER FINE AND COARSE RANGES

VEFAHREN UND VORRICHTUNG ZUM EINSTELLEN VON TAKTSIGNALEN UBER FEIN- UND GROBBEREICHE

PROCEDE ET APPAREIL DE REGLAGE DE TEMPORISATION DE SIGNAUX DANS DES PLAGES FINES ET GROSSIERES

PATENT ASSIGNEE:

MICRON TECHNOLOGY, INC., (1177696), 8000 South Federal Way, P.O. Box 6,
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INVENTOR:

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MANNING, Troy, A., 8153 South Obadiah Lane, Meridian, ID 83642, (US)

LEGAL REPRESENTATIVE:

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Winzererstrasse 106, 80797 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 1016086 A1 000705 (Basic)

EP 1016086 B1 021127

WO 99014759 990325

APPLICATION (CC, No, Date): EP 98949381 980918; WO 98US19575 980918

PRIORITY (CC, No, Date): US 933324 970918

DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI;

LU; MC; NL; PT; SE

INTERNATIONAL PATENT CLASS: G11C-007/00; H03K-005/13

NOTE:

No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200248	1677
CLAIMS B	(German)	200248	1421
CLAIMS B	(French)	200248	1858
SPEC B	(English)	200248	11358
Total word count - document A			0
Total word count - document B			16314
Total word count - documents A + B			16314

...SPECIFICATION c command packets that contain both control and address information. Data is coupled between the processor 702 and the memory devices 10a-c, through the **memory controller** 705 and a data **bus portion** of the processor bus 704. The **memory controller** 705 applies write data from the processor 702 to the memory devices 10a-c, and it applies read data from the memory devices 10a-c...

9/3,K/14 (Item 14 from file: 348)
DIALOG(R) File 348:EUROPEAN PATENTS
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00914584

Signal-transfer system and semiconductor device for high speed data transfer

Signalübertragungssystem und Halbleitervorrichtung für Hochgeschwindigkeitsdatenübertragung

Système de transfert de signaux et circuit à semi-conducteur pour le transfert de données à grande vitesse

PATENT ASSIGNEE:

FUJITSU LIMITED, (211463), 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588, (JP), (Applicant designated States: all)

INVENTOR:

Okajima, Yoshinori, c/o Fujitsu Limited, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211, (JP)

Higuchi, Tsuyoshi, c/o Fujitsu Limited, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211, (JP)

LEGAL REPRESENTATIVE:

Stebbing, Timothy Charles et al (59641), Haseltine Lake & Co., Imperial House, 15-19 Kingsway, London WC2B 6UD, (GB)

PATENT (CC, No, Kind, Date): EP 834814 A2 980408 (Basic)
EP 834814 A3 001220

APPLICATION (CC, No, Date): EP 97301864 970319;

PRIORITY (CC, No, Date): JP 96262126 961002

DESIGNATED STATES: DE; GB

EXTENDED DESIGNATED STATES: AL; LT; LV; RO; SI

INTERNATIONAL PATENT CLASS: G06F-013/40

ABSTRACT WORD COUNT: 66

NOTE:

Figure number on first page: 2

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9815	1712
SPEC A	(English)	9815	6940
Total word count - document A			8652
Total word count - document B			0
Total word count - documents A + B			8652

...SPECIFICATION can be made smaller. Here, the terminology "skew" means a displacement in signal-reception timing. If a single long loop is put in place without **dividing** the **bus**, a signal output from the **memory controller** 40 goes clockwise round the bus to arrive at a given memory at a different time from when a signal going counterclockwise round the

bus...this configuration, the memories 31-1 through 31-8 can be arranged at 1-cm intervals without being affected by a physical size of the **memory controller 30**.

In Fig.14B, the **bus 33** is **divided** into a **bus 33A** and a **bus 33B**, and each of the buses 33A and 33B is folded in two, with a memory controller 30A having two input...

...a configuration, the memories 31-1 through 31-8 can be arranged at 1-cm intervals without being affected by a physical size of the **memory controller 30A**. Further, since the **bus 33** is **divided** into the **buses 33A** and **33B** to shorten the bus length, skews at reception ends can be reduced by suppressing an influence of signals reflected at the bus...

9/3,K/15 (Item 15 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00635737

Fully pipelined and highly concurrent memory controller
Speichersteuereinheit mit hohem Grade der Gleichzeitigkeit und Arbeitsteilung

Contrôleur mémoire hautement concurrent et pleinement parallèle

PATENT ASSIGNEE:

Compaq Computer Corporation, (687791), 20555 FM 149, Houston Texas 77070, (US), (Proprietor designated states: all)

INVENTOR:

Landry, John A., 16318 Avenplace Road, Tomball, Texas 77375, (US)
Santeler, Paul A., 13211 Mistyhill Drive, Cypress, Texas 77429, (US)
Thome, Gary W., 16406 Marrat Court, Tomball, Texas 77075, (US)
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Collins, Michael J., 16030 Lakestone Drive, Tombal, Texas 77375, (US)

LEGAL REPRESENTATIVE:

Brunner, Michael John et al (28871), GILL JENNINGS & EVERY Broadgate House 7 Eldon Street, London EC2M 7LH, (GB)

PATENT (CC, No, Kind, Date): EP 617365 A1 940928 (Basic)
EP 617365 B1 010613

APPLICATION (CC, No, Date): EP 94302014 940322;

PRIORITY (CC, No, Date): US 34290 930322

DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; IE; IT; LI; NL; SE

INTERNATIONAL PATENT CLASS: G06F-013/16

ABSTRACT WORD COUNT: 247

NOTE:

Figure number on first page: 4

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	2086
CLAIMS B	(English)	200124	2197
CLAIMS B	(German)	200124	1904
CLAIMS B	(French)	200124	2642
SPEC A	(English)	EPABF2	26481
SPEC B	(English)	200124	26662
Total word count - document A			28572
Total word count - document B			33405
Total word count - documents A + B			61977

...CLAIMS for determining whether an operation cycle on said processor bus is directed to said plurality of memory devices or said host bus device; and

a **memory controller** connected to said processor, host and memory control **bus portions**, to said data buffer, to said means for transferring addresses between said processor and host buses, to said operation cycle direction determination means and to...controls said means connected to said input/output and host address bus portions to transfer addresses between said input/output and host buses,

wherein said **memory controller** controls said means connected to said processor and host address **bus portions** for transferring addresses between said processor and host buses to transfer addresses between said processor and host buses when said memory controller detects said bus...

...CLAIMS MD) data bus portions for transferring data between said buses, said data buffer having control inputs for receiving signals controlling transfers between said buses;

a **memory controller** (156) connected to said processor, host and memory control **bus portions**, to said data buffer, to said means for transferring addresses between said processor and host buses, to said operation cycle direction determination means and to...

9/3,K/16 (Item 16 from file: 348)
DIALOG(R) File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

00483660

Memory access bus arrangement
Busanordnung fur Speicherzugriff
Dispositif de bus d'accès a memoire
PATENT ASSIGNEE:

AT&T Corp., (589370), 32 Avenue of the Americas, New York, NY 10013-2412,
(US), (applicant designated states: DE;ES;FR;GB;IT)

INVENTOR:

Laha, Subhasis, 4320 Nutmeg Lane, Apt. 230, Lisle, Illinois 60532, (US)
Thompson, Dennis Joseph, 1815 Allen Drive, Geneva, Illinois 60134, (US)

LEGAL REPRESENTATIVE:

Buckley, Christopher Simon Thirsk et al (28912), Lucent Technologies (UK)
Ltd, 5 Mornington Road, Woodford Green, Essex IG8 0TU, (GB)

PATENT (CC, No, Kind, Date): EP 458516 A2 911127 (Basic)
EP 458516 A3 920408
EP 458516 B1 971105

APPLICATION (CC, No, Date): EP 91304338 910515;

PRIORITY (CC, No, Date): US 529051 900525

DESIGNATED STATES: DE; ES; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-013/16;

ABSTRACT WORD COUNT: 180

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9710W5	1363
CLAIMS B	(German)	9710W5	1287
CLAIMS B	(French)	9710W5	1486
SPEC B	(English)	9710W5	4279
Total word count - document A			0
Total word count - document B			8415
Total word count - documents A + B			8415

...SPECIFICATION wherein a processor accesses a bus at one interval and reserves an access on that bus during a second interval for the response from a **memory controller**. Both the **split** transaction arrangement and the pipeline **bus** are considerably more expensive than a tenured bus and continue to have substantial limitations on the total throughput of the bus thus creating a bottleneck...

9/3,K/19 (Item 3 from file: 349)
DIALOG(R) File 349:PCT FULLTEXT
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00848836

Image available

MECHANISM FOR EFFICIENT SCHEDULING OF COMMUNICATION FLOWS
MECANISME D'ORDONNANCEMENT EFFICACE DE FLUX DE COMMUNICATION

Patent Applicant/Assignee:

SUN MICROSYSTEMS INC, 901 San Antonio Road, Palo Alto, CA 94303, US, US
(Residence), US (Nationality)

Inventor(s):

WARD Kenneth A, 5 Joyce Circle, Shrewsbury, MA 01545, US,

Legal Representative:

KOWERT Robert C (agent), Conley, Rose & Tayon, P.C., P.O. Box 398,
Austin, TX 78767-0398, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200182528 A2-A3 20011101 (WO 0182528)

Application: WO 2001US13105 20010423 (PCT/WO US0113105)

Priority Application: US 2000553966 20000421

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ

DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ

LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG

SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 7093

Fulltext Availability:

Detailed Description

Detailed Description

... also be coupled to host bus 103 and shared by CPUs 102. Alternatively,
or additionally, each CPU 102 may have its own local memory and **memory
controller**. A host channel adapter 108 couples the host **bus elements**
to various YO resources. Host channel adapter 108 may be integrated in a
single component with memory controller 106. A switch 1 1 0 may...

9/3,K/20 (Item 4 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00783398 **Image available**

CIRCUIT AND METHOD FOR A MULTIPLEXED REDUNDANCY SCHEME IN A MEMORY DEVICE

CIRCUIT ET PROCEDE POUR PLAN DE REDONDANCE MULTIPLEXEE DANS UNE MEMOIRE

Patent Applicant/Assignee:

MICRON TECHNOLOGY INC, 8000 South Federal Way, Boise, ID 83707, US, US
(Residence), US (Nationality)

Inventor(s):

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WRIGHT Jeffrey P, 425 Cotterell Drive, Boise, ID 83709, US,

Legal Representative:

BULCHIS Edward W (et al) (agent), Dorsey & Whitney LLP, Suite 3400, 1420
Fifth Avenue, Seattle, WA 98101, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200116955 A1 20010308 (WO 0116955)

Application: WO 2000US23726 20000829 (PCT/WO US0023726)

Priority Application: US 99387650 19990901

Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK

DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR

LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ

TM TR TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 6704

Fulltext Availability:
Detailed Description

Detailed Description

... devices 106a-c via the system memory bus 123 by sending the memory devices 106a-c control and address information. Data is coupled between the **memory controller** 108 and the memory devices 106a-c through a data **bus portion** of the system memory bus 113. During a read operation, data is transferred from the memory devices 106a-c over the memory bus 113 to...

9/3,K/21 (Item 5 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00757092 **Image available**

SYSTEM AND ADAPTER CARD FOR REMOTE CONSOLE EMULATION

SYSTEME ET CARTE ADAPTATEUR POUR EMULATION DE CONSOLES A DISTANCE

Patent Applicant/Assignee:

UNISYS CORPORATION, Township Line and Union Meeting Roads, P.O. Box 500,
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Inventor(s):

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Legal Representative:

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P.O. Box 500, Blue Bell, PA 19424-0001, US

Patent and Priority Information (Country, Number, Date):

Patent: WO 200070472 A1 20001123 (WO 0070472)

Application: WO 2000US12308 20000505 (PCT/WO US0012308)

Priority Application: US 99310542 19990512

Designated States: BR JP

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Publication Language: English

Filing Language: English

Fulltext Word Count: 10803

Fulltext Availability:

Detailed Description

Detailed Description

... that the processor 26 executes is stored, and an associated local random-access memory 40, both of which interface to the processor 26 via local **bus segment** 28b. A **memory controller** 36, such as a Direct Memory Access controller (DMA), may also be interfaced to the bus segment 28b to control memory transfers to and from...

9/3,K/22 (Item 6 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00569827 **Image available**

METHOD AND APPARATUS FOR HIGH SPEED DATA CAPTURE USING BIT-TO-BIT TIMING CORRECTION, AND MEMORY DEVICE USING SAME

PROCEDE ET APPAREIL DE CAPTURE RAPIDE DE DONNEES UTILISANT UNE CORRECTION DE SYNCHRONISATION BIT A BIT ET DISPOSITIF A MEMOIRE LES UTILISANT

Patent Applicant/Assignee:

MICRON TECHNOLOGY INC,

Inventor(s):

KEETH Brent,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200033200 A1 20000608 (WO 0033200)

Application: WO 99US27877 19991124 (PCT/WO US9927877)

Priority Application: US 98201519 19981130

Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE

ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT
LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT
UA UG UZ VN YU ZA ZW GH GM KE LS MW SD SL SZ TZ UG ZW AM AZ BY KG KZ MD
RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF
CG CI CM GA GN GW ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 24667

Fulltext Availability:

Detailed Description

Detailed Description

... memory bus 23 by sending the memory devices 16a- I 6c command packets that contain both control and address information. Data are coupled between the **memory controller** 18 and the memory devices 16a-16c through a data **bus portion** of the system memory bus 23. During a read operation, data is transferred from the packetized memory devices 16a-16c over the memory bus 23...

9/3,K/23 (Item 7 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00566667 **Image available**

ADVANCED DEFERRED SHADING GRAPHICS PIPELINE PROCESSOR
PROCESSEUR PIPELINE GRAPHIQUE EVOLUE A OMBRAGE DIFFERE

Patent Applicant/Assignee:

APPLE COMPUTER INC, 1 Infinite Loop, Cupertino, CA 95014-2084, US, US
(Residence), US (Nationality)

Inventor(s):

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ARNOLD Vaughn T, 621 Canepa Drive, Scotts Valley, CA 95066, US,
BENKUAL Jack, 11661 Timber Spring Court, Cupertino, CA 95014, US,
BRATT Joseph P, 1045 Oaktree Drive, San Jose, CA 95129, US,
CUAN George, 798 Lusterleaf Drive, Sunnyvale, CA 94086, US,
DODGEN Steven L, 15735 Forest Hill Drive, Boulder Creek, CA 95006, US,
FANG Emerson S, 1197 Wisteria Drive, Fremont, CA 94539, US,
GONG Zhaoyu G, 1342 S. Stelling Road, Cupertino, CA 95014, US,
HO Thomas Y, 40732 Ondina Place, Fremont, CA 94539, US,
HSU Hengwei, 4209 Canfield Drive, Fremont, CA 94536, US,
LI Sidong, 5598 LeFevre Drive, San Jose, CA 95118, US,
NG Sam, 34377 Maybird Circle, Fremont, CA 94555, US,
PAPAKIPOS Matthew N, 1701 Oak Avenue, Menlo Park, CA 94025, US,
REDGRAVE Jason R, 278 Martens Avenue, Mountain View, CA 95040, US,
TRIVEDI Sushma S, 1208 Rembrandt Drive, Sunnyvale, CA 94087, US,
TUCK Nathan D, 8666 Somerset Avenue, San Diego, CA 92123, US,
GO Shun Wai, 370 Sandhurst Drive, Milpitas, CA 95035, US,
FUNG Lindy, 358 Pescadero Terrace, Sunnyvale, Ca 94086, US,
NGUYEN Tuan D, 5327 Birch Grove Drive, San Jose, CA 95123, US,
GRASS Joseph P, 357 Lennox Avenue, Menlo Park, CA 94025, US,
HONG Bor-Shyue, 2325 Oak Flat Road, San Jose, CA 95131, US,
MAMMEN Abraham, 2780 Lylewood Drive, Pleasanton, CA 94588, US,
RASHID Abbas, 34369 Eucalyptus Terrace, Fremont, CA 94555-1982, US,
TSAY Albert Suan-Wei, 38129 Cambridge Court, Fremont, CA 94536, US,

Legal Representative:

ANANIAN R Michael (et al) (agent), Flehr Hohbach Test Albritton & Herbert
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Patent and Priority Information (Country, Number, Date):

Patent: WO 200030040 A1 20000525 (WO 0030040)

Application: WO 99US18971 19990820 (PCT/WO US9918971)

Priority Application: US 9897336 19980820; US 98213990 19981217

Designated States: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE

ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT

LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT

UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW SD SL SZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English
Filing Language: English
Fulltext Word Count: 180456

Fulltext Availability:
Detailed Description

Detailed Description

... 2015 Consumed Mode - Bump Packet (BMP) Data Bus
2016 Consumed Mode - Light Color Packet (LITC) Command Bus
2017 Consumed Mode - Light Color Packet (LITC) Data Bus
2018 Consumed Mode - Light State Packet (LITS) Command Bus
2019 Consumed Mode - Light State Packet (LITS) Data Bus
2020 Consumed Mode - Matrix Packet (MTX) Command Bus
2021 Consumed Mode - Matrix Packet (MTX) Data Bus...

9/3,K/24 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00512761

INCREASING THE MEMORY PERFORMANCE OF FLASH MEMORY DEVICES BY WRITING
SECTORS SIMULTANEOUSLY TO MULTIPLE FLASH MEMORY DEVICES
AMELIORATION DE LA VITESSE DE LA MEMOIRE DANS UN DISPOSITIF A MEMOIRE FLASH
AU MOYEN D'UNE OPERATION D'ENREGISTREMENT EXECUTEE SIMULTANEMENT SUR
DES DISPOSITIFS MULTIPLES

Patent Applicant/Assignee:

LEXAR MEDIA INC,
ESTAKHRI Petro,
IMAN Berhanu,

Inventor(s):

ESTAKHRI Petro,
IMAN Berhanu,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9944113 A2 19990902
Application: WO 99US4247 19990225 (PCT/WO US9904247)
Priority Application: US 9830697 19980225

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES
FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD
MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US
UZ VN YU ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT
BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA
GN GW ML MR NE SN TD TG

Publication Language: English
Fulltext Word Count: 16151

Fulltext Availability:
Claims

Claim

... bytes of said odd sector;
said memory bus includes,
a first split bus coupled to transmit said even data bytes of said
sectors between said **memory**
controller and said first memory unit;
a second **split bus** coupled to transmit said odd data bytes of said
sectors between said **memory controller** and said second memory unit.

4 A memory storage device as...bytes of a
second sector;
said memory bus includes,
a first split bus coupled to transmit (least significant ?) data bytes of
said sectors between said

memory controller and said first memory unit;
a second **split bus** coupled to transmit (most significant ?) data
bytes of said sectors between said memory controller and said second
memory unit.

13 A memory storage device as...

9/3,K/25 (Item 9 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00505506 **Image available**
DATA TRANSFERRING IN SOURCE-SYNCHRONOUS AND COMMON CLOCK PROTOCOLS
TRANSFERT DE DONNEES SELON DES PROTOCOLES DE TRANSMISSION DE SOURCE
SYNCHRONES ET A HORLOGE COMMUNE

Patent Applicant/Assignee:

INTEL CORPORATION,
MACWILLIAMS Peter D,
WU William S,
SAMPATH Dilip K,
PRASAD Bindi A,

Inventor(s):

MACWILLIAMS Peter D,
WU William S,
SAMPATH Dilip K,
PRASAD Bindi A,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9936858 A1 19990722
Application: WO 99US199 19990105 (PCT/WO US9900199)
Priority Application: US 986322 19980113

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK
DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ
LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK
SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ
BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT
SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 6448

Fulltext Availability:
Detailed Description

Detailed Description

... latter case. The data phase occurs only if a transaction requires a
data transfer. The data phase can be response initiated (for example, by
the **memory controller** or another processor) or request initiated.

The **bus** accommodates deferred transactions by **splitting** a **bus**
transaction into two independent transactions. The first transaction
involves a request by a requesting agent and a response by the responding
agent. The response includes...

9/3,K/26 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00488434 **Image available**
METHOD AND APPARATUS FOR COUPLING SIGNALS BETWEEN TWO CIRCUITS OPERATING IN
DIFFERENT CLOCK DOMAINS
PROCEDE ET DISPOSITIF DE COUPLAGE DE SIGNAUX ENTRE DEUX CIRCUITS
FONCTIONNANT DANS DES DOMAINES DE SYNCHRONISATION DIFFERENTS

Patent Applicant/Assignee:

MICRON TECHNOLOGY INC,

Inventor(s):

MANNING Troy A,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9919786 A1 19990422
Application: WO 98US21582 19981013 (PCT/WO US9821582)
Priority Application: US 97948712 19971010
Designated States: AL AM AT AU BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI
GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW
MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN YU GH GM KE
LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR
GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 11015
Fulltext Availability:
Detailed Description

Detailed Description

... c command packets that contain both control and address information. Data is coupled between the processor 302 and the memory devices 20a-c, through the **memory controller** 305 and a data **bus portion** of the processor bus 304. The **memory controller** 305 applies write data from the processor 302 to the memory devices 20a-c, and it applies read data from the memory devices 20a-c...

9/3,K/27 (Item 11 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00483407 **Image available**

METHOD AND APPARATUS FOR ADJUSTING THE TIMING OF SIGNALS OVER FINE AND COARSE RANGES **PROCEDE ET APPAREIL DE REGLAGE DE TEMPORISATION DE SIGNAUX DANS DES PLACES FINES ET GROSSIERES**

Patent Applicant/Assignee:

MICRON TECHNOLOGY INC,

Inventor(s):

KEETH Brent,

MANNING Troy A,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9914759 A1 19990325

Application: WO 98US19575 19980918 (PCT/WO US9819575)

Priority Application: US 97933324 19970918

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES
FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD
MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ
VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH
CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW
ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 17696

Fulltext Availability:
Detailed Description

Detailed Description

... c command packets that contain both control and address information. Data is coupled between the processor 702 and the memory devices 10a-c, through the **memory controller** 705 and a data **bus portion** of the processor bus 704. The **memory controller** 705 applies write data from the processor 702 to the memory devices 10a-c, and it applies read data from the 15 memory devices...

9/3,K/28 (Item 12 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00468833 **Image available**

METHOD AND APPARATUS FOR SWITCHING BETWEEN SOURCE-SYNCHRONOUS AND COMMON
CLOCK DATA TRANSFER MODES IN A MULTIPLE AGENT PROCESSING SYSTEM
PROCEDE ET APPAREIL PERMETTANT D'EFFECTUER LA COMMUTATION ENTRE UN MODE DE
TRANSFERT DE DONNEES SYNCHRONE PAR RAPPORT A LA SOURCE ET UN MODE DE
TRANSFERT DE DONNEES FONDE SUR UNE HORLOGE COMMUNE DANS UN SYSTEME DE
TRAITEMENT A PLUSIEURS AGENTS

Patent Applicant/Assignee:

INTEL CORPORATION,
PAWLOWSKI Stephen S,
MACWILLIAMS Peter D,
WU William S,
SCHULTZ Len J,

Inventor(s):

PAWLOWSKI Stephen S,
MACWILLIAMS Peter D,
WU William S,
SCHULTZ Len J,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9859298 A1 19981230
Application: WO 98US13339 19980625 (PCT/WO US9813339)
Priority Application: US 97881941 19970625

Designated States: AL AM AT AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE
DK DK EE EE ES FI FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK
LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL
TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG
KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF
BJ CF CG CI CM GA GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 7277

Fulltext Availability:

Detailed Description

Detailed Description

... latter case. The data phase occurs only if a transaction
requires a data transfer. The data phase can be response initiated (for
example, by the **memory controller** or another processor) or request
initiated

The **bus** accommodates deferred transactions by **splitting** a **bus**
transaction into two independent transactions. The first transaction
involves a request by a requesting agent and a response by the
responding agent. The response includes...

9/3,K/29 (Item 13 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

(c) 2003 WIPO/Univentio. All rts. reserv.

00424418 **Image available**

METHOD AND APPARATUS FOR CHANGING DATA TRANSFER WIDTHS IN A COMPUTER SYSTEM
PROCEDE ET DISPOSITIF DE MODIFICATION DES LARGEURS DE TRANSFERT DE DONNEES

Patent Applicant/Assignee:

INTEL CORPORATION,

Inventor(s):

PAWLOWSKI Stephen S,
MACWILLIAMS Peter D,
SINGH Gurbir,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9814880 A1 19980409
Application: WO 97US13400 19970728 (PCT/WO US9713400)
Priority Application: US 96723572 19960930

Designated States: AL AM AT AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE
DK DK EE EE ES FI FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT
LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM TR
TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM

AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA
GN ML MR NE SN TD TG

Publication Language: English
Fulltext Word Count: 10592
Fulltext Availability:
Detailed Description

Detailed Description

... latter case. The data phase occurs only if a transaction requires a data transfer. The data phase can be response initiated (for example, by the **memory controller** or another processor) or request initiated.

The **bus** accommodates deferred transactions by **splitting** a **bus** transaction into two independent transactions. The first transaction involves a request by a requesting agent and a response by the responding agent. The response includes...

9/3,K/30 (Item 14 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00419889 **Image available**

A DATA FLOW CONTROL MECHANISM FOR A BUS SUPPORTING TWO-AND THREE-AGENT
TRANSACTIONS
LOGIQUE DE GESTION DES FLUX DE DONNEES POUR UN BUS ACCEPTANT DES
TRANSACTIONS A DEUX ET TROIS AGENTS

Patent Applicant/Assignee:
INTEL CORPORATION,

Inventor(s):
MACWILLIAMS Peter D,
SARANGDHAR Nitin V,
PAWLOWSKI Stephen S,
SINGH Gurbir,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9810350 A1 19980312
Application: WO 97US11419 19970630 (PCT/WO US9711419)
Priority Application: US 96709215 19960906

Designated States: AL AM AT AT AU AZ BA BB BG BR BY CA CH CN CU CZ CZ DE DE
DK DK EE EE ES FI FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT
LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM TR
TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM
AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA
GN ML MR NE SN TD TG

Publication Language: English
Fulltext Word Count: 7831

Fulltext Availability:
Detailed Description

Detailed Description

... laiter case. Thv data phase occurs only ii'a transaction requires a data transfer. The data phase can be response Initiated (for exaniple, by the **memory controller** orailcither processor) or request initiated.

- M The **bus** acconinli3dates deferred transactions by **splitting** a **bus** transaction into two independent transactions. The first transaction involves a request by a requesting agent and a response by the responding agent. In one embodiment...

9/3,K/31 (Item 15 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00418760 **Image available**

METHOD AND APPARATUS FOR SUPPORTING MULTIPLE OVERLAPPING ADDRESS SPACES ON
A SHARED BUS

PROCEDE ET APPAREIL DE SUPPORT D'ESPACES D'ADRESSES A PLUSIEURS
CHEVAUchemENTS SUR UN BUS COMMUN

Patent Applicant/Assignee:

INTEL CORPORATION,

Inventor(s):

McWILLIAMS Peter D,

PAWLOWSKI Stephen S,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9809221 A1 19980305

Application: WO 97US11632 19970701 (PCT/WO US9711632)

Priority Application: US 96705684 19960829

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DE

DK DK EE EE ES FI FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT

LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SK SL TJ TM TR

TT UA UG UZ VN YU ZW GH KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM

AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA

GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 7771

Fulltext Availability:

Detailed Description

Detailed Description

... latter case. The data phase occurs only if a transaction requires a data transfer. The data phase can be response initiated (for example, by the **memory controller** or another processor) or request initiated.

The **bus** accommodates deferred transactions by **splitting** a **bus** transaction into two independent transactions. The first transaction involves a request by a requesting agent and a response by the responding agent. In one embodiment...

9/3,K/32 (Item 16 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00357150

MEMORY CONTROLLER FOR BOTH INTERLEAVED AND NON-INTERLEAVED MEMORY

REGISSEUR DE MEMOIRE POUR MEMOIRE AVEC ET SANS ENTRELACEMENT

Patent Applicant/Assignee:

APPLE COMPUTER INC,

Inventor(s):

NUNZIATA Ann B,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9639664 A1 19961212

Application: WO 96US8496 19960603 (PCT/WO US9608496)

Priority Application: US 95470971 19950606

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CZ DE DK EE ES FI GB

GE HU IL IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ

PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AM

AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT

SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 8348

Fulltext Availability:

Detailed Description

Detailed Description

... each or a 12 bit row address and a 10 bit column address. Each of the row and column address bits is supplied to the **memory controller** 20 over the system **bus** portion 50. In the exemplary embodiment of Figure 2, address bits numbered 26 through 2 are supplied to memory controller 20 which provide sufficient information to...

9/3,K/33 (Item 17 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2003 WIPO/Univentio. All rts. reserv.

00353664 **Image available**

**MULTIPLE SEQUENCE MPEG DECODER AND PROCESS FOR CONTROLLING SAME
DECODEUR MPEG A SEQUENCE MULTIPLE ET PROCESSUS DE COMMANDE**

Patent Applicant/Assignee:

THE 3DO COMPANY,

Inventor(s):

WASSERMAN Steve C,

BALDWIN James Armand,

MITSUOKA George,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9636178 A1 19961114

Application: WO 96US6510 19960508 (PCT/WO US9606510)

Priority Application: US 95439085 19950510; US 95440464 19950510

Designated States: AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB

GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL

PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AM AZ

BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 18262

Fulltext Availability:

Claims

Claim

... and the motion video output
it DMA controller.

65. An MPEG decoding system, comprising:

a host system including a host system memory, a

host system **memory controller**, a host system processor

and a host system **bus**, the host system memory being

divided into at least a storage area buffer, a first

and a second display buffer buffers, a coded data

11/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

01234045

SYSTEM AND ADAPTER CARD FOR REMOTE CONSOLE EMULATION
SYSTEM UND ADAPTERKARTE FUR EMULATION EINER ENTFERNTEN KONSOLE
SYSTEME ET CARTE ADAPTATEUR POUR EMULATION DE CONSOLES A DISTANCE
PATENT ASSIGNEE:

UNISYS CORPORATION, (842794), Township Line and Union Meeting Roads P.O.
Box 500, Blue Bell, PA 19424-0001, (US), (Proprietor designated states:
all)

INVENTOR:

POWDERLY, Terrence, V., 10 Crown Lane, East Fallowfield, PA 19320, (US)

LEGAL REPRESENTATIVE:

Modiano, Guido, Dr.-Ing. et al (40786), Modiano, Josif, Pisanty & Staub,
Baaderstrasse 3, 80469 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 1190329 A1 020327 (Basic)

EP 1190329 B1 030312

WO 2000070472 001123

APPLICATION (CC, No, Date): EP 2000928862 000505; WO 2000US12308 000505

PRIORITY (CC, No, Date): US 310542 990512

DESIGNATED STATES (Pub A): AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE;

IT; LI; LU; MC; NL; PT; SE; (Pub B): CH; DE; GB; LI

EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI

INTERNATIONAL PATENT CLASS: G06F-013/10

NOTE:

No A-document published by EPO

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200311	920
CLAIMS B	(German)	200311	847
CLAIMS B	(French)	200311	990
SPEC B	(English)	200311	7952
Total word count - document A			0
Total word count - document B			10709
Total word count - documents A + B			10709

...SPECIFICATION controller 24 is isolated on a separate local bus segment 28a. Because of this isolation, network traffic will not add load to the main local bus segment 28 over which the graphics controller 22 communicates with the processor 26 and host I/O bus 20. It is understood, however, that in other embodiments, one or both of the...First, the processor 26 configures the local bus segment 28a (a secondary PCI bus), as well as the bridges 32 and 34. The network interface controller 24 is then initialized on the bus segment 28a as a LOCAL device (i.e., not visible to the host CPU 50). The graphics controller BIOS (which in this example is a VGA BIOS) is loaded next into the host memory 52 by the host BIOS. The processor 26...

11/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

00869423

Hardware assist for YUV data format conversion to software MPEG decoder
Hardwarehilfe fur MPEG-Dekodierungssoftware zur YUV-Datenformatumwandlung
Assistance materielle a un logiciel de decodage MPEG pour la conversion de
format de donnees YUV

PATENT ASSIGNEE:

Cirrus Logic, Inc., (1079711), 3100 West Warren Avenue, M/S 521, Fremont,
California 94538-6423, (US), (applicant designated states:

AT;BE;CH;DE;FR;GB;IE;LI;NL)

INVENTOR:

Keene, David, 48 Northam Ave., San Carlos, CA 94070, (US)

LEGAL REPRESENTATIVE:

Lundquist, Arne (23591), Oxoen 1:9, 139 50 Vaermdoe, (SE)
 PATENT (CC, No, Kind, Date): EP 797181 A2 970924 (Basic)
 EP 797181 A3 980107
 APPLICATION (CC, No, Date): EP 97104446 970315;
 PRIORITY (CC, No, Date): US 619203 960321
 DESIGNATED STATES: AT; BE; CH; DE; FR; GB; IE; LI; NL
 INTERNATIONAL PATENT CLASS: G09G-001/16; G09G-005/02;
 ABSTRACT WORD COUNT: 125
 LANGUAGE (Publication,Procedural,Application): English; English; English
 FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9709W3	919
SPEC A	(English)	9709W3	5703
Total word count - document A			6622
Total word count - document B			0
Total word count - documents A + B			6622

...SPECIFICATION above that 768 kilobytes available for a video buffer.
 Display controller 320 may then read a separate areas of display memory 130 for video and **graphics** portions of a display **image** , as the two areas may be in different color spaces (e.g., 8 bpp for **graphics** , 24 bpp for video), as is known in the art. When YUV data is transferred to display memory 130, the first Y address for a...
 ...512 kilobytes of Y values may be effectively expanded by the address translation scheme to double that, or one kilobyte of address space. Thus, display **controller** may **divide** an address from PCI **bus** 150 by two from where it would go in the frame buffer to take care of that address translation.
 352 bytes of Y data may...

11/3,K/4 (Item 4 from file: 348)
 DIALOG(R)File 348:EUROPEAN PATENTS
 (c) 2003 European Patent Office. All rts. reserv.

00767419

Single-chip microcomputer

Einchip-Mikrocomputer

Micro-ordinateur monopuce

PATENT ASSIGNEE:

HITACHI, LTD., (204144), 6, Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo 100, (JP), (applicant designated states: DE;FR;GB;IT)

HITACHI MICROCOMPUTER SYSTEM LTD., (1298040), 5-22-1, Josuihon-cho, Kodaira-shi, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT)

INVENTOR:

Kawasaki, Shumpei, 2-28-4, Matsugaoka, Nakano-ku, Tokyo, (JP)

Akao, Yasushi, 6-14-39, Higashikoigakubo, Kokubunji-shi, Tokyo, (JP)

Noguchi, Kouki, 3-23-18, Kamikitazawa, Setagaya-ku, Tokyo, (JP)

Hasegawa, Atsushi, 7-5-11, Fujimi-cho, Tachikawa-shi, Tokyo, (JP)

Ohsuga, Hiroshi, 2-15-3, Minamidaira, Hino-shi, Tokyo, (JP)

Kurakazu, Keiichi, 5003-12, Kamiyamaguchi, Tokorozawa-shi, Saitama, (JP)

Matsubara, Kiyoshi, 2-3-11-210, Misumi-cho, Higashimurayama-shi, Tokyo, (JP)

Hayakawa, Akio, 726-3, Yotsuya-machi, Hachiouji-shi, Tokyo, (JP)

Ito, Yoshitaka, 3-2-40, Gakuenhigashi-cho, Kodaira-shi, Tokyo, (JP)

LEGAL REPRESENTATIVE:

Strehl Schubel-Hopf Groening & Partner (100941), Maximilianstrasse 54, 80538 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 718779 A1 960626 (Basic)

APPLICATION (CC, No, Date): EP 96102998 940810;

PRIORITY (CC, No, Date): JP 93255099 930917; JP 9436742 940209

DESIGNATED STATES: DE; FR; GB; IT

RELATED PARENT NUMBER(S) - PN (AN):

EP 646873 (EP 941125205)

INTERNATIONAL PATENT CLASS: G06F-013/42; G06F-013/40; G06F-015/78;

ABSTRACT WORD COUNT: 175

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	66
SPEC A	(English)	EPAB96	30322
Total word count - document A			30388
Total word count - document B			0
Total word count - documents A + B			30388

...ABSTRACT bus having a central processing unit and a cache memory connected therewith; a second bus having a dynamic memory access control circuit and an external bus interface connected therewith; a break controller for connecting the first bus and the second bus selectively; a third bus having a peripheral module connected therewith and having a lower-speed bus cycle than the bus cycles...

...at a high speed. Moreover, the peripheral module required to have no operation speed is isolated so that the power dissipation can be reduced. (see image in original document) ...

...SPECIFICATION bus together with the cache memory; the divider unit connected with the second bus together with the dynamic memory access control circuit and the external bus interface; the break controller connected with the first and second buses and having the bus transceiver function ...for effecting the signal transfers and the synchronization between the second bus and the third bus. As a resultant effect, a high-speed three-dimensional image processing can be realized by the relatively simple construction.

Although our invention has been specifically described in connection with its embodiments, it should not be...bus together with the cache memory; the divider unit connected with the second bus together with the dynamic memory access control circuit and the external bus interface; the break controller connected with the first and second buses and having the bus transceiver function to connect the address bus of the first bus selectively with the...controller for effecting the signal transfers and the synchronization between the second bus and the third bus. As a result, a high-speed three-dimensional image processing can be realized by the relatively simple construction. ...

11/3,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00767418

Single-chip microcomputer

Einchip-Mikrocomputer

Micro-ordinateur monopuce

PATENT ASSIGNEE:

HITACHI, LTD., (204144), 6, Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo 100, (JP), (applicant designated states: DE;FR;GB;IT)

HITACHI MICROCOMPUTER SYSTEM LTD., (1298040), 5-22-1, Josuihon-cho, Kodaira-shi, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT)

INVENTOR:

Kawasaki, Shumpei, 2-28-4, Matsugaoka, Nakano-ku, Tokyo, (JP)

Akao, Yasushi, 6-14-39, Higashikoigakubo, Kokubunji-shi, Tokyo, (JP)

Noguchi, Kouki, 3-23-18, Kamikitazawa, Setagaya-ku, Tokyo, (JP)

Hasegawa, Atsushi, 7-5-11, Fujimi-cho, Tachikawa-shi, Tokyo, (JP)

Ohsuga, Hiroshi, 2-15-3, Minamidaira, Hino-shi, Tokyo, (JP)

Kurakazu, Keiichi, 5003-12, Kamiyamaguchi, Tokorozawa-shi, Saitama, (JP)

Matsubara, Kiyoshi, 2-3-11-210, Misumi-cho, Higashimurayama-shi, Tokyo, (JP)

Hayakawa, Akio, 726-3, Yotsuya-machi, Hachioji-shi, Tokyo, (JP)

Ito, Yoshitaka, 3-2-40, Gakuenhigashi-cho, Kodaira-shi, Tokyo, (JP)

LEGAL REPRESENTATIVE:

Strehl Schubel-Hopf Groening & Partner (100941), Maximilianstrasse 54, 80538 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 718768 A1 960626 (Basic)

APPLICATION (CC, No, Date): EP 96102994 940810;
PRIORITY (CC, No, Date): JP 93255099 930917; JP 9436472 940209
DESIGNATED STATES: DE; FR; GB; IT
RELATED PARENT NUMBER(S) - PN (AN):
EP 646873 (EP 941125205)
INTERNATIONAL PATENT CLASS: G06F-012/08; G06F-015/78;
ABSTRACT WORD COUNT: 175

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	114
SPEC A	(English)	EPAB96	30323
Total word count - document A			30437
Total word count - document B			0
Total word count - documents A + B			30437

...ABSTRACT bus having a central processing unit and a cache memory connected therewith; a second bus having a dynamic memory access control circuit and an external **bus** interface connected therewith; a **break controller** for connecting the first **bus** and the second bus selectively; a third bus having a peripheral module connected therewith and having a lower-speed bus cycle than the bus cycles...

...at a high speed. Moreover, the peripheral module required to have no operation speed is isolated so that the power dissipation can be reduced. (see **image** in original document) ...

...SPECIFICATION bus together with the cache memory; the divider unit connected with the second bus together with the dynamic memory access control circuit and the external **bus** interface; the **break controller** connected with the first and second buses and having the bus transceiver function ...for effecting the signal transfers and the synchronization between the second bus and the third bus. As a resultant effect, a high-speed three-dimensional **image** processing can be realized by the relatively simple construction.

Although our invention has been specifically described in connection with its embodiments, it should not be...bus together with the cache memory; the divider unit connected with the second bus together with the dynamic memory access control circuit and the external **bus** interface; the **break controller** connected with the first and second buses and having the bus transceiver function to connect the address bus of the first bus selectively with the...controller for effecting the signal transfers and the synchronization between the second bus and the third bus. As a result, a high-speed three-dimensional **image** processing can be realized by the relatively simple construction. ...

11/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

00674272

Single-chip microcomputer.

Einchip-Mikrorechner.

Micro-ordinateur monopuce.

PATENT ASSIGNEE:

HITACHI, LTD., (204144), 6, Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo 100, (JP), (applicant designated states: DE;FR;GB;IT)

HITACHI MICROCOMPUTER SYSTEM LTD., (1298040), 5-22-1, Josuihon-cho, Kodaira-shi, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT)

INVENTOR:

Kawasaki, Shumpei, 2-28-4, Matsugaoka, Nakano-ku, Tokyo, (JP)

Akao, Yasushi, 6-14-39, Higashikoigakubo, Kokubunji-shi, Tokyo, (JP)

Noguchi, Kouki, 3-23-18, Kamikitazawa, Setagaya-ku, Tokyo, (JP)

Hasegawa, Atsushi, 7-5-11, Fujimi-cho, Tachikawa-shi, Tokyo, (JP)

Ohsuga, Hiroshi, 2-15-3, Minamidara, Hino-shi, Tokyo, (JP)

Kurakazu, Keiichi, 5003-12, Kamiyamaguchi, Tokorozawa-shi, Saitama, (JP)

Matsubara, Kiyoshi, 2-3-11-210, Misumi-cho, Higashimurayama-shi, Tokyo, (JP)

Hayakawa, Akio, 726-3, Yotsuya-machi, Hachiouji-shi, Tokyo, (JP)

Ito, Yoshitaka, 3-2-40, Gakuenhigashi-cho, Kodaira-shi, Tokyo, (JP)

LEGAL REPRESENTATIVE:

Strehl Schubel-Hopf Groening & Partner (100941), Maximilianstrasse 54, D-80538 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 646873 A2 950405 (Basic)

EP 646873 A3 950920

APPLICATION (CC, No, Date): EP 94112520 940810;

PRIORITY (CC, No, Date): JP 93255099 930917; JP 9436472 940209

DESIGNATED STATES: DE; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-013/40; G06F-015/78; G06F-012/08;

G06F-013/42;

ABSTRACT WORD COUNT: 152

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
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CLAIMS A	(English)	EPAB95	907
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SPEC A	(English)	EPAB95	30325
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Total word count - document A	31232
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Total word count - document B	0
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Total word count - documents A + B	31232
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...ABSTRACT bus having a central processing unit and a cache memory connected therewith; a second bus having a dynamic memory access control circuit and an external **bus** interface connected therewith; a **break controller** for connecting the first **bus** and the second bus selectively; a third bus having a peripheral module connected therewith and having a lower-speed bus cycle than the bus cycles...

...at a high speed. Moreover, the peripheral module required to have no operation speed is isolated so that the power dissipation can be reduced. (see **image** in original document)

...SPECIFICATION bus together with the cache memory; the divider unit connected with the second bus together with the dynamic memory access control circuit and the external **bus** interface; the **break controller** connected with the first and second buses and ...for effecting the signal transfers and the synchronization between the second bus and the third bus. As a resultant effect, a high-speed three-dimensional **image** processing can be realized by the relatively simple construction.

Although our invention has been specifically described in connection with its embodiments, it should not be...bus together with the cache memory; the divider unit connected with the second bus together with the dynamic memory access control circuit and the external **bus** interface; the **break controller** connected with the first and second buses and having the bus transceiver function to connect the address bus of the first bus selectively with the...controller for effecting the signal transfers and the synchronization between the second bus and the third bus. As a result, a high-speed three-dimensional **image** processing can be realized by the relatively simple construction. ...

11/3,K/7 (Item 7 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00598740

Personal computer with SCSI bus power control.

Peronalrechner mit SCSI-Bus Versorgungsspannungssteuerung.

Ordinateur personnel avec controle d'alimentation du bus SCSI.

PATENT ASSIGNEE:

INTERNATIONAL BUSINESS MACHINES CORPORATION, (200125), Old Orchard Road, Armonk, N.Y. 10504, (US), (applicant designated states: DE;FR;GB)

INVENTOR:

Keener, Don Steven, 1019 West Royal Palm Road, Boca Raton, Florida 33486,

(US)

Moore, Gregory James, 8371 Huntsman Place, Boca Raton, Florida 33433,

(US)

Stine, Eric Speestra, 500 Egret Circle No.8306, Delray Beach, Florida 33444, (US)

LEGAL REPRESENTATIVE:

Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)

PATENT (CC, No, Kind, Date): EP 588469 A1 940323 (Basic)

APPLICATION (CC, No, Date): EP 93304414 930607;

PRIORITY (CC, No, Date): US 947011 920917

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-013/40; G05F-001/577; H02H-009/02;

ABSTRACT WORD COUNT: 168

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	232
SPEC A	(English)	EPABF2	2519
Total word count - document A			2751
Total word count - document B			0
Total word count - documents A + B			2751

...ABSTRACT bus with a first portion for operative interconnection of the SCSI controller with any SCSI devices connected through a planar board and a second SCSI bus portion for operative interconnection of the SCSI controller with any SCSI devices mounted remotely from the planar board. A power supply for supplying electrical power to any SCSI devices operatively connected to the SCSI controller by either of the first and second SCSI bus portions has a thermistor for limiting the current drawn by any SCSI devices operatively connected to the SCSI controller by either of the bus portions and a pair of diodes each for isolating a respective corresponding portion of the SCSI bus. (see image in original document)

11/3,K/8 (Item 8 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00598281

Multi-processor video display apparatus.

Video-Anzeigegerat mit einem Mehrprozessor.

Appareil d'affichage video a processeur multiple.

PATENT ASSIGNEE:

Koninklijke Philips Electronics N.V., (200769), Groenewoudseweg 1, 5621 BA Eindhoven, (NL), (applicant designated states: DE;FR;GB;IT)

INVENTOR:

Johnson, Brian, c/o Int. Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven, (NL)

Epstein, Michael, c/o Int. Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven, (NL)

LEGAL REPRESENTATIVE:

Strijland, Wilfred et al (21291), INTERNATIONAAL OCTROOIBUREAU B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven, (NL)

PATENT (CC, No, Kind, Date): EP 605054 A2 940706 (Basic)

EP 605054 A3 960207

APPLICATION (CC, No, Date): EP 93203690 931224;

PRIORITY (CC, No, Date): US 998358 921230

DESIGNATED STATES: DE; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-015/16; H04N-005/14; G06T-001/20;

G06F-017/50; G06F-015/80;

ABSTRACT WORD COUNT: 266

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
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CLAIMS A	(English)	EPABF2	837
SPEC A	(English)	EPABF2	4327
Total word count	- document A		5164
Total word count	- document B		0
Total word count	- documents A + B		5164

...SPECIFICATION consist of a register for storing a received data packet and a tristate buffer which controls the transmission of such data packet on the relevant **bus segment**. A series of programmable bus interconnection **controllers** are respectively coupled to the respective **bus segments**, each of which controls the bus latch for the corresponding bus segment and determines from the headers of data packets arriving at such latch to which of the sequential video **images** the arriving packets relate. The controllers are programmed so that each serial one thereof selects the packets for a corresponding serial one of the successive video **images** in each successive group of a predetermined number of such **images**, and permits other packets to proceed downstream to the bus latch of the next bus segment. A series of data processors are respectively coupled to the respective **bus segments** and associated **controllers**, each for receiving from its **bus segment** all of the data packets relating to a respective video **image** selected by the relevant controller. Each data processor is programmed to process the data packets of the selected **image** in accordance with the applicable signal processing algorithm and to supply the processed packets back to the bus segment for transmission on the bus, such transmission being synchronized by the relevant controller. The number N of data processors is such that processing of all data packets relating to each video **image** is completed by the processor assigned to that **image** within the time period of N video **images**, so that each successive series of N video **images** can be cyclically assigned by the successive controllers to the series of data processors. Thus, the data processors respectively process in parallel the data packets of respective entire video **images** of the video picture. An output interface, which is a logic circuit similar to the input interface, receives the processed data packets at the output...

...CLAIMS real time display of the video picture corresponding to a selected signal processing algorithm, as applied to a digital video signal representing time sequential video **images** which constitute the video picture; said apparatus comprising:

- at least one input interface means for receiving the video signal and assembling the data therein for each of the sequential video **images** into successive data packets in successive equal time slots, each data packet including a header identifying the video **image** to which a data packet relates;
- a data bus for receiving the successive data packets and transmitting them downstream along said bus;
- a series of...

...said bus for operationally segmenting it into successive segments between which transmission is controlled by the intervening bus latch;

- a series of programmable bus interconnection **controllers** respectfully coupled to the respective **bus segments**, each **controller** being adapted to control the bus latch of the associated **bus segment** and to determine from the headers of data packets received at such bus latch those of such data packets which are for a particular video **image**; said controllers being programmed so that each serial one thereof selects the data packets for a corresponding serial one of the successive video **images** in each successive series of a predetermined number N of the serial video **images**;
- a series of at least said number N of data processors respectively coupled to the respective **bus segments** and the corresponding **controllers**, each for receiving from its **bus segment** all of the data packets for the video **image** selected by the relevant controller and being programmed to process such data packets in accordance with said selected processing algorithm, each data processor supplying the processed data packets produced thereby back to its **bus segment** for transmission thereon as synchronized

by the relevant **controller** ;

each data processor being adapted to complete processing of the data packets for its selected video **image** during the time period of said series of N video **images** , so that each successive series of N video **images** is cyclically assigned by said series of controllers to said series of data processors for processing in parallel of the data packets of respective complete video **images** of the video picture; and

at least one output interface means for receiving from said bus the processed data packets of the successive video **images** and assembling such processed data packets into an output digital video signal;

whereby said output digital signal is adapted to produce on a video display...

11/3,K/9 (Item 9 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00489889

Bus architecture for a multimedia system

Busarchitektur fur ein Multimediansystem

Architecture de bus pour un systeme multimedia

PATENT ASSIGNEE:

International Business Machines Corporation, (200120), Old Orchard Road, Armonk, N.Y. 10504, (US), (Proprietor designated states: all)

INVENTOR:

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Freeman, Bobby Joe, 1381 SW 29th Avenue, Boynton Beach, Florida 33426, (US)

Suarez, Gustave Armando, 21482 Woodchuck Lane, Boca Raton, Florida 33428, (US)

Wilkie, Bruce James, 15635 Lindbergh Lane, West Palm Beach, Florida 33414, (US)

LEGAL REPRESENTATIVE:

Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)

PATENT (CC, No, Kind, Date): EP 493881 A2 920708 (Basic)

EP 493881 A3 921230

EP 493881 B1 950920

EP 493881 B2 000426

APPLICATION (CC, No, Date): EP 91310693 911120;

PRIORITY (CC, No, Date): US 625577 901211

DESIGNATED STATES: DE; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-003/14; G09G-005/00

ABSTRACT WORD COUNT: 66

NOTE:

Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200017	480
CLAIMS B	(German)	200017	499
CLAIMS B	(French)	200017	604
SPEC B	(English)	200017	12384
Total word count - document A			0
Total word count - document B			13967
Total word count - documents A + B			13967

...SPECIFICATION a system display. Colley, Martin, "Parallel-Architecture Windowing Display" Department of Computer Science, University of Essex, Wivenhoe Park, Colchester, Essex, U.K. (1987) discloses such a system.

In Colley, the window modules are provided by **dividing** a display memory into physically separate window areas. **Each image** signal window is maintained in its entirety in a respective window module; the

visibility of overlapping portions of the windows is determined via arbitration as...

11/3,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00489888

Multimedia system
Multimedienssystem
Systeme multimedia
PATENT ASSIGNEE:

International Business Machines Corporation, (200120), Old Orchard Road,
Armonk, N.Y. 10504, (US), (Proprietor designated states: all)

INVENTOR:

Dinwiddie, John Monroe, Jr., 112 Pacer Circle, West Palm Beach, Florida
33414, (US)

Freeman, Bobby Joe, 1381 SW 28th Avenue, Boynton Beach, Florida 33426,
(US)

Suarez, Gustave Armando, 21482 Woodchuck Lane, Boca Raton, Florida 33428,
(US)

Wilkie, Bruce James, 15635 Lindbergh Lane, West Palm Beach, Florida 33414
, (US)

LEGAL REPRESENTATIVE:

Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual
Property Department Hursley Park, Winchester Hampshire SO21 2JN, (GB)

PATENT (CC, No, Kind, Date): EP 492795 A2 920701 (Basic)
EP 492795 A3 921230
EP 492795 B1 950920
EP 492795 B2 000426

APPLICATION (CC, No, Date): EP 91310692 911120;

PRIORITY (CC, No, Date): US 625564 901211

DESIGNATED STATES: DE; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-003/14; G09G-005/00

ABSTRACT WORD COUNT: 101

NOTE:

Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200017	414
CLAIMS B	(German)	200017	408
CLAIMS B	(French)	200017	484
SPEC B	(English)	200017	12373
Total word count - document A			0
Total word count - document B			13679
Total word count - documents A + B			13679

...SPECIFICATION a system display. Colley, Martin, "Parallel-Architecture
Windowing Display" Department of Computer Science, University of Essex,
Wivenhoe Park, Colchester, Essex, U.K. (1987) discloses such a system.

In Colley, the window modules are provided by dividing a display
memory into physically separate window areas. Each image signal
window is maintained in its entirety in a respective window module; the
visibility of overlapping portions of the windows is determined via
arbitration as...

11/3,K/11 (Item 11 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00299763

Programmable controller with multiple task processors.
Speicherprogrammierbare Steuerung mit mehreren Taskprozessoren.
Automate programmable avec plusieurs processeurs de taches.

PATENT ASSIGNEE:

ALLEN-BRADLEY COMPANY, INC., (204331), 1201 South Second Street,
Milwaukee Wisconsin 53204, (US), (applicant designated states: FR)

INVENTOR:

Flood, Mark A., 1330 Worton Avenue, Mayfield Heights Ohio 44124, (US)
Kalan, Michael D., 1245 Jackie Lane, Mayfield Heights Ohio 44124, (US)
Preis, Peter N., 5212 Spencer Road, Lyndhurst Ohio 44124, (US)
Peterson, Alden L., 1671 West 5th Street/Second Floor, Brooklyn New York
11223, (US)

LEGAL REPRESENTATIVE:

Lippert, Hans, Dipl.-Ing. et al (7781), Reichel und Reichel Parkstrasse
13, D-60322 Frankfurt, (DE)

PATENT (CC, No, Kind, Date): EP 311007 A2 890412 (Basic)
EP 311007 A3 890802
EP 311007 B1 940309

APPLICATION (CC, No, Date): EP 88116390 881004;

PRIORITY (CC, No, Date): US 105815 871007

DESIGNATED STATES: FR

INTERNATIONAL PATENT CLASS: G05B-019/04;

ABSTRACT WORD COUNT: 148

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	565
CLAIMS B	(German)	EPBBF1	507
CLAIMS B	(French)	EPBBF1	618
SPEC B	(English)	EPBBF1	19079
Total word count - document A			0
Total word count - document B			20769
Total word count - documents A + B			20769

...SPECIFICATION the functional modules of the programmable controller 10
will be described in detail in the following sections.

System Controller

As noted previously, the system controller **module** 16 provides a
communication interface for the programmable controller to external
terminals and local area networks. The system controller 16 also performs
system housekeeping functions...

...in the corresponding program execution module 18 is updated. For
example, this includes adding, deleting and changing various rungs of the
ladder program.

The system **controller** as shown schematically in Figure 3 connects to
the backplane **buses** 21-23 and is **divided** into three sections
(delineated **by** dashed lines) for backplane interface, processing and
communication operations. The backplane interface section supervises the
backplane access for all the rack modules and interfaces the...

11/3,K/12 (Item 12 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00237935

Multiprocessor system.

Multiprozessorsystem.

Systeme a multiprocesseur.

PATENT ASSIGNEE:

HITACHI, LTD., (204141), 6, Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo
101, (JP), (applicant designated states: DE;FR;GB)

INVENTOR:

Ueda, Hirotada, 22-49, Nishimachi-2-chome, Kokubunji-shi, (JP)
Kato, Kanji, 5297-5-4, Oaza Yamaguchi, Tokorozawa-shi, (JP)
Matsushima, Hitoshi, 13-18, Sunagawacho-1-chome, Tachikawa-shi, (JP)

LEGAL REPRESENTATIVE:

Strehl, Schubel-Hopf, Groening (100941), Maximilianstrasse 54 Postfach 22
14 55, W-8000 Munchen 22, (DE)

PATENT (CC, No, Kind, Date): EP 236762 A1 870916 (Basic)

EP 236762 B1 920520
APPLICATION (CC, No, Date): EP 87101820 870210;
PRIORITY (CC, No, Date): JP 8651236 860308
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-015/66; G06F-015/16;
ABSTRACT WORD COUNT: 109

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	667
CLAIMS B	(German)	EPBBF1	541
CLAIMS B	(French)	EPBBF1	839
SPEC B	(English)	EPBBF1	5697
Total word count - document A			0
Total word count - document B			7744
Total word count - documents A + B			7744

...SPECIFICATION and data to an external image output unit (not shown)
flow. Local memories 2 are to store data flowing on the ring bus 1.
Processor **elements** 3 implement **image** data processing by executing the
program. Path **controllers** 4, each connected between a processor element
3 and a local memory 2, are also connected serially in a shift register
fashion.

Each processor element...

11/3,K/14 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00781825

SYSTEM OF REUSABLE SOFTWARE PARTS AND METHODS OF USE
SYSTEME D'UNITES LOGICIELLES REUTILISABLES ET PROCEDES D'UTILISATION

Patent Applicant/Assignee:

Z-FORCE CORPORATION, 151 Kalmus Drive, Suite B-250, Costa Mesa, CA 92626,
US, US (Residence), US (Nationality)

Inventor(s):

MILOUSHEV Vladimir I, 30802 Calle Barbosa, Laguna Niguel, CA 92677, US,
NICKOLOV Peter A, 158 Giotto, Irvine, CA 92614, US,

Legal Representative:

TACHNER Adam H (et al) (agent), Crosby, Heafey, Roach & May, Suite 2000,
Two Embarcadero Center, San Francisco, CA 94111, US,

Patent and Priority Information (Country, Number, Date):

Patent: WO 200114959 A2-A3 20010301 (WO 0114959)

Application: WO 2000US22694 20000816 (PCT/WO US0022694)

Priority Application: US 99149371 19990816; US 99149624 19990816

Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ

DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ

LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG

SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW

(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English

Filing Language: English

Fulltext Word Count: 182432

Fulltext Availability:

Detailed Description

Detailed Description

... a virtual property container, DM-VPC

Figure 126 illustrates a hierarchical repository, DM-REP

Figure 127 Illustrates the binary structure of the DM-REP serialized
image

Figure 128 illustrates a parameterizer from registry, DM

PRM

.Figure 129 illustrates a serializer to registry, DM-SER
Figure 130 illustrates the internal structure of...

...DM P2E

Figure 134 illustrates a property setter adapter, DM-PSET
Figure 135 illustrates an eight property setters adapter, DM-PSET8
Figure 136 illustrates a **graphical** representation of a dynamic container for parts
Figure 1 37 illustrates types of connections between contained objects and objects outside of the container that the...table interface to event interface, the adapters have an option by which return data from the outgoing event may be copied to the original operation **bus** before returning from the call.

11. Boundary

1 1. 1. Terminals (DM-NP2D)

Terminal "in" with direction "In" and contract [-POLY. Note: All operations on...

11/3,K/15 (Item 3 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00757092 **Image available**

SYSTEM AND ADAPTER CARD FOR REMOTE CONSOLE EMULATION

SYSTEME ET CARTE ADAPTATEUR POUR EMULATION DE CONSOLES A DISTANCE

Patent Applicant/Assignee:

UNISYS CORPORATION, Township Line and Union Meeting Roads, P.O. Box 500,
Blue Bell, PA 19424-0001, US, US (Residence), US (Nationality)

Inventor(s):

POWDERLY Terrence V, 10 Crown Lane, East FallowField, PA 19320, US

Legal Representative:

STARR Mark T, Unisys Corporation, Township Line and Union Meeting Roads,
P.O. Box 500, Blue Bell, PA 19424-0001, US

Patent and Priority Information (Country, Number, Date):

Patent: WO 200070472 A1 20001123 (WO 0070472)

Application: WO 2000US12308 20000505 (PCT/WO US0012308)

Priority Application: US 99310542 19990512

Designated States: BR JP

(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Publication Language: English

Filing Language: English

Fulltext Word Count: 10803

Fulltext Availability:

Detailed Description

Detailed Description

... controller 24 is isolated on a separate local bus segment 28a. Because of this isolation, network traffic will not add load to the main local **bus segment** 28 over which the **graphics controller** 22 communicates with the processor 26 and host I/O bus 20. It is understood, however, that in other embodiments, one or both of the...processor 26 configures the local bus segment 28a (a secondary PCI bus), as well as the 1 5 bridges 32 and 34. The network interface **controller** 24 is then initialized on the **bus segment** 28a as a LOCAL device (i.e., not visible to the host CPU 50). The **graphics controller BIOS** (which in this example is a VGA BIOS) is loaded next into the host memory 52 by the host BIOS. The processor 26...

11/3,K/16 (Item 4 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00353664 **Image available**

**MULTIPLE SEQUENCE MPEG DECODER AND PROCESS FOR CONTROLLING SAME
DECODEUR MPEG A SEQUENCE MULTIPLE ET PROCESSUS DE COMMANDE**

Patent Applicant/Assignee:

THE 3DO COMPANY,

Inventor(s):

WASSERMAN Steve C,

BALDWIN James Armand,

MITSUOKA George,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9636178 A1 19961114

Application: WO 96US6510 19960508 (PCT/WO US9606510)

Priority Application: US 95439085 19950510; US 95440464 19950510

Designated States: AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB

GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL

PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AM AZ

BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 18262

Fulltext Availability:

Claims

Claim

... the motion video output
it DMA controller.

65. An MPEG decoding system, comprising:
a host system including a host system memory, a
host system memory **controller**, a host system processor
and a host system **bus**, the host system memory being
divided into at least a storage area buffer, a first
and a second display buffer buffers, a coded data
buffer, and a first and second reference buffers;
MPEG video data decoding hardware including:
means for parsing **image** data blocks and
motion vector blocks from macroblock data;
means for constructing motion vector data
from coded motion vector blocks;
means for performing entropy decoding on
coded **image** data blocks;
means for performing inverse quantization of
the coded **image** data blocks;
means for taking the inverse discrete cosine
transform of the coded **image** data;
a motion compensation means, coupled to the
means for taking the inverse discrete cosine
transform and the motion vector processor, and
operatively coupled to the system memory, for
constructing picture data from the **image** data and
motion vector blocks;
a video output DMA controller, operatively
coupled to the system memory controller and the
motion compensation means;
a video output...

...memory and the video output DMA controller;
and
instruction means, provided in the storage area
and executable by the host system processor, for
directing encoded **image** data to the parsing means in a
decoding order, for configuring the means for parsing
image data blocks, and interacting with the host system
memory to store decoded **image** data, display **image** data,
and configuration data for the

DIALOG(R)File 349:PCT FULLTEXT
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00352658 **Image available**

CONTROLLER FOR PROVIDING ACCESS TO A VIDEO FRAME BUFFER IN A SPLIT-BUS TRANSACTION ENVIRONMENT

CONTROLEUR DONNANT ACCES A UN TAMPON D'IMAGES DANS UN ENVIRONNEMENT DE TRANSACTIONS SUR BUS DEDOUBLE

Patent Applicant/Assignee:

APPLE COMPUTER INC,

Inventor(s):

CHILDERS Brian A,

BADEN Eric A,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9635172 A1 19961107

Application: WO 96US4263 19960327 (PCT/WO US9604263)

Priority Application: US 95434197 19950503

Designated States: AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB
GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL
PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AM AZ
BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 5418

Fulltext Availability:

Detailed Description

Detailed Description

**CONTROLLER FOR PROVIDING ACCESS TO A VIDEO
FRAME BUFFER IN A SPLIT - BUS TRANSACTION ENVIRONMENT
BACKGROUND**

The present invention relates to **graphics controllers**, and more particularly to means within a **graphics** controller for accessing a video frame buffer in response to an access request received by means of a system bus

having split-bus transaction capability...capability environment. This can be appreciated by examining the prior art strategy for

handling frame buffer read requests that would be used by the **graphics controller 111** if the system **bus 101** had **split - bus** transaction capability. Referring to the flow chart of FIG. 2, the process starts when the **graphics controller 111** receives a frame buffer read request from a requesting agent that is connected to the system bus 101 (now presumed to be a "**split response bus**", i.e., one having **split - bus** transaction capability) (step 201). The **graphics controller 111** must now begin the arbitration process to obtain access to the frame buffer 117 and initiate the desired read (step 203). The **graphics controller 111** must also request access to the system data bus (step 205), so that the data will have a place to go when it...a **graphics controller** connected to a tightly ordered system bus; FIG. 2 is a flow chart illustrating the detrimental effects of applying prior

art **graphics controller** techniques in a **split -response bus** environment;

FIG. 3 is a block diagram of a computer system in which the present invention is utilized;

FIG. 4 is a block diagram of the overall data flow within the inventive bridge/ **graphics controller**; and

FIG. 5 is a flow chart of steps performed by a **graphics controller** in accordance

11/3,K/18 (Item 6 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00210151 **Image available**

APPARATUS AND METHOD FOR WRITING AND READING DIGITAL INFORMATION

·
APPAREIL ET PROCEDE D'ECRITURE ET DE LECTURE D'INFORMATIONS NUMERIQUES

Patent Applicant/Assignee:

PRIMOV Beni,

Inventor(s):

PRIMOV Beni,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9207356 A1 19920430

Application: WO 91AU480 19911016 (PCT/WO AU9100480)

Priority Application: AU 9064686 19901016

Designated States: AT AU BB BE BF BG BJ BR CA CF CG CH CI CM DE DK ES FI FR

GA GB GN GR HU IT JP KP KR LK LU MC MG ML MR MW NL NO PL RO SD SE SE SN

SU TD TG US

Publication Language: English

Fulltext Word Count: 4687

Fulltext Availability:

Detailed Description

Claims

Detailed Description

... until a command to stop reading is received.

According to a further aspect of this invention there is provided an apparatus for producing a photographic **image** of digital information on a rotatable disk having at least one light sensitive surface, comprising an intelligent controller connected to a data bus; at least...

...outputs; each

bank of fibre outputs consisting of coloured optical fibres or including coloured filters; the arrangement being such that digital information from said data **bus** is **split** into groups of fixed numbers of bits by said intelligent **controller**, -said groups of bits being used as addresses for said digital information; the laser light and addresses being routed through said optical routing means to...

Claim

... outputs; each

bank of fibre outputs consisting of coloured optical fibres or including coloured filters; the arrangement being such that digital information from said data **bus** is **split** into groups of fixed numbers of bits by said intelligent **controllerr** said groups of bits being used as addresses for said digital information; the laser light and addresses being routed through said optical routing means to...

12/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

00767419

Single-chip microcomputer

Einchip-Mikrocomputer

Micro-ordinateur monopuce

PATENT ASSIGNEE:

HITACHI, LTD., (204144), 6, Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo
100, (JP), (applicant designated states: DE;FR;GB;IT)

HITACHI MICROCOMPUTER SYSTEM LTD., (1298040), 5-22-1, Josuihon-cho,
Kodaira-shi, Tokyo, (JP), (applicant designated states: DE;FR;GB;IT)

INVENTOR:

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LEGAL REPRESENTATIVE:

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80538 Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 718779 A1 960626 (Basic)

APPLICATION (CC, No, Date): EP 96102998 940810;

PRIORITY (CC, No, Date): JP 93255099 930917; JP 9436742 940209

DESIGNATED STATES: DE; FR; GB; IT

RELATED PARENT NUMBER(S) - PN (AN):

EP 646873 (EP 941125205)

INTERNATIONAL PATENT CLASS: G06F-013/42; G06F-013/40; G06F-015/78;

ABSTRACT WORD COUNT: 175

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	66
SPEC A	(English)	EPAB96	30322
Total word count - document A			30388
Total word count - document B			0
Total word count - documents A + B			30388

...SPECIFICATION and to reduce the power dissipation of the bus drive circuit.

The second internal bus is composed of an address bus AB2 and a data bus DB2 and connected with the divider unit DIVU, the dynamic memory access controller DMAC and an external bus interface OBIF. When an access to the aforementioned cache memory is a miss hit, the central processing unit CPU has...

...the dynamic memory access controller DMAC may be caused by a program miss to garble the content of the data memory CDM of the cache memory .

In this embodiment, a break controller UBC coupled between the aforementioned first internal bus and second internal bus is utilized to solve the aforementioned problem such as the miss hit...that high-speed operations may be accomplished by making accesses while holding the word lines of the individual RAMs in the selected state through the bus state controller RSC.

The break controller UBC is connected with the first internal bus (AB1, DB1) and the second internal bus (AB2, DB2) to make comparison with the addresses set in...

...break of the data, which is caused as a result that the dynamic memory access controller DMAC erroneously writes the address stored in the

cache **memory** . In short, merely by **dividing** the internal bus to speed up the internal circuit and to reduce the power dissipation, such a fatal defect of the system can be eliminated as might otherwise be caused without the treatment of this embodiment to allow the data of the cache **memory** to be **broken** and inaccessible from the central processing unit CPU.

Fig. 7 is a block diagram showing one embodiment of the aforementioned bus state controller BSC. This...out of the cache data being selected in parallel is fetched by the central processing unit CPU. If a miss hit occurs, an external main **memory** is accessed through the aforementioned **break controller** UBC and external **bus** interface.

In Fig. 17, the cache control register CCR has control bits for cache enabling, instruction fill inhibiting, data fill inhibiting, two-way mode and...single-chip microcomputer which comprises: the central processing unit and the multiply and accumulate arithmetic unit connected with the first bus together with the cache **memory** ; the **divider** unit connected with the second bus together with the dynamic memory access control circuit and the external **bus** interface; the **break controller** connected with the first and second buses and having the bus transceiver function ...single-chip microcomputer which comprises: the central processing unit and the multiply and accumulate arithmetic unit connected with the first bus together with the cache **memory** ; the **divider** unit connected with the second bus together with the dynamic memory access control circuit and the external **bus** interface; the **break controller** connected with the first and second buses and having the bus transceiver function to connect the address bus of the first bus selectively with the...

12/3,K/3 (Item 3 from file: 348)
DIALOG(R) File 348:EUROPEAN PATENTS
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00742380

Data processor with set associative unit
Datenprozessor mit Teilassoziativer Einheit
Processeur de donnees a unite associative par jeux
PATENT ASSIGNEE:

Hitachi, Ltd., (204144), 6, Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo,
(JP), (Proprietor designated states: all)

INVENTOR:

Yoshioka, Shinichi, c/o Hitachi Semiconductor US, 179 East Tasman Drive,
San Jose, CA 95134, (US)
Kawasaki, Ikuya, 1-398-13, Ogawa-machi, Kodaira-shi,, Tokyo,, (JP)
Narita, Susumu,, 1-21-70, Higashitokura, Kokubunji-shi,, Tokyo,, (JP)
Tamaki, Saneaki,, 1-59-2-b-315, Onta-cho, Higashimurayama-shi,, Tokyo,,
(JP)

LEGAL REPRESENTATIVE:

Strehl Schubel-Hopf & Partner (100941), Maximilianstrasse 54, 80538
Munchen, (DE)

PATENT (CC, No, Kind, Date): EP 701212 A2 960313 (Basic)
EP 701212 A3 970226
EP 701212 B1 030115

APPLICATION (CC, No, Date): EP 95114249 950911;

PRIORITY (CC, No, Date): JP 94241992 940909; JP 9587555 950320; JP 95240873
950825

DESIGNATED STATES: DE; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-012/10; G06F-012/08

ABSTRACT WORD COUNT: 141

NOTE:

Figure number on first page: 2

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	490
CLAIMS B	(English)	200303	656
CLAIMS B	(German)	200303	553

CLAIMS B	(French)	200303	714
SPEC A	(English)	EPAB96	23066
SPEC B	(English)	200303	23253
Total word count - document A			23560
Total word count - document B			25176
Total word count - documents A + B			48736

...SPECIFICATION omitted in Fig. 13.

In Fig. 13, the system bus (S-bus) is connected to the central processing unit CPU, multiplier MLT, cache unit CACHE, **memory** management unit MMU and user **break controller** UBC. The cache bus (C-bus) is connected to the cache memory CACHE, **memory** management unit MMU, instruction **break controller** UBC and bus state **controller** BCS. The peripheral bus (P-bus), coupled to the bus state controller BSC, is connected to such built-in peripheral modules as the timer TMU ...the miss is read from the external memory MMRY. The data or instruction thus read is retained as a new cache entry in the cache **memory** CACHE-M.

The user **break controller** UBC is furnished to reinforce the debugging function of the embodiment. This **controller** checks to see if the state of the system bus (S-bus) matches the **break** condition in question. In the event of a match, the user break controller UBC generates a break interrupt to the central processing unit CPU. The...

...SPECIFICATION omitted in Fig. 13.

In Fig. 13, the system bus (S-bus) is connected to the central processing unit CPU, multiplier MLT, cache unit CACHE, **memory** management unit MMU and user **break controller** UBC. The cache bus (C-bus) is connected to the cache memory CACHE, **memory** management unit MMU, instruction **break controller** UBC and bus state **controller** BCS. The peripheral bus (P-bus), coupled to the bus state controller BSC, is connected to such built-in peripheral modules as the timer TMU...

...the miss is read from the external memory MMRY. The data or instruction thus read is retained as a new cache entry in the cache **memory** CACHE-M.

The user **break controller** UBC is furnished to reinforce the debugging function of the embodiment. This **controller** checks to see if the state of the system bus (S-bus) matches the **break** condition in question. In the event of a match, the user break controller UBC generates a break interrupt to the central processing unit CPU. The...

12/3,K/4 (Item 4 from file: 348)
 DIALOG(R) File 348:EUROPEAN PATENTS
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00702747

Reconfigurable ASIC.

Wiederkonfigurierbare anwendungsspezifische integrierte Schaltung.

Circuit integre d'application specifique (ASIC) reconfigurable.

PATENT ASSIGNEE:

Pilkington Micro-Electronics (DSP) Limited, (1905840), Prescott Road, St. Helens, Merseyside WA10 3TT, (GB), (applicant designated states: AT; BE; CH; DE; DK; ES; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE)

INVENTOR:

Austin, Kenneth, Brockhurst Hall, Brockhurst Way, Northwich, Cheshire, CW9 8AL, (GB)

LEGAL REPRESENTATIVE:

Cardwell, Stuart Martin et al (52502), Roystons Tower Building Water Street, Liverpool, Merseyside L3 1BA, (GB)

PATENT (CC, No, Kind, Date): EP 668659 A2 950823 (Basic)

APPLICATION (CC, No, Date): EP 95301002 950216;

PRIORITY (CC, No, Date): GB 9403030 940217

DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE

INTERNATIONAL PATENT CLASS: H03K-019/177;

ABSTRACT WORD COUNT: 170

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	921
SPEC A	(English)	EPAB95	4762
Total word count - document A			5683
Total word count - document B			0
Total word count - documents A + B			5683

...SPECIFICATION as multiplier expansion cells. The columns in each block are headed up by decode cells.

Referring now to Figure 15, the configurable static random access **memory** (SRAM) 3 stores **partition** data passed to it from the sequencer and **controller** 5 along **partition** data **bus** 72. The operation of the DSP requires the storing and retrieving of data and the provision of the SRAM on the device ensures that access...

12/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

00527118

Computer system with a cache memory.

Rechneranordnung mit Cachespeicher.

Systeme d'ordinateur a antememoire.

PATENT ASSIGNEE:

Kabushiki Kaisha Toshiba, (213137), 72, Horikawa-cho Saiwai-ku,
Kawasaki-shi, (JP), (applicant designated states: DE;FR;GB)

INVENTOR:

Yamaki, Kazunori, c/o Intellectual Property Div., K.K. Toshiba, 1-1
Shibaura 1-chome, Minato-ku, Tokyo 105, (JP)

LEGAL REPRESENTATIVE:

Henkel, Feiler, Hanzel & Partner (100401), Mohlstrasse 37, W-8000 Munchen
80, (DE)

PATENT (CC, No, Kind, Date): EP 535537 A2 930407 (Basic)
EP 535537 A3 930421

APPLICATION (CC, No, Date): EP 92116385 920924;

PRIORITY (CC, No, Date): JP 91278598 910930; JP 91278600 910930

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-012/08;

ABSTRACT WORD COUNT: 96

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	664
SPEC A	(English)	EPABF1	4210
Total word count - document A			4874
Total word count - document B			0
Total word count - documents A + B			4874

...SPECIFICATION unit and controls data transfer between the two. When, for example, CPU 1 gets access to ROM 30 connected to the system bus, the system **controller** 20 transfers, via the data **bus** 37 in two **divided** portions, data which has been read out of ROM 30. Further, the system controller 20 supplies, via the data bus 24 to CPU 1, 32 bit data which has been read, as the two **divided** portions, out of **ROM** 30.

Now let it be assumed that, in such a system, CPU 1 can execute memory access to an address space corresponding to addresses A31...

12/3,K/7 (Item 7 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

00489889

Bus architecture for a multimedia system

Busarchitektur fur ein Multimediansystem
Architecture de bus pour un systeme multimedia

PATENT ASSIGNEE:

International Business Machines Corporation, (200120), Old Orchard Road,
Armonk, N.Y. 10504, (US), (Proprietor designated states: all)

INVENTOR:

Dinwiddie, John Monroe, Jr., 112 Pacer Circle, West Palm Beach, Florida
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Freeman, Bobby Joe, 1381 SW 29th Avenue, Boynton Beach, Florida 33426,
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Suarez, Gustavo Armando, 21482 Woodchuck Lane, Boca Raton, Florida 33428,
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Wilkie, Bruce James, 15635 Lindbergh Lane, West Palm Beach, Florida 33414
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LEGAL REPRESENTATIVE:

Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual
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PATENT (CC, No, Kind, Date): EP 493881 A2 920708 (Basic)

EP 493881 A3 921230

EP 493881 B1 950920

EP 493881 B2 000426

APPLICATION (CC, No, Date): EP 91310693 911120;

PRIORITY (CC, No, Date): US 625577 901211

DESIGNATED STATES: DE; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-003/14; G09G-005/00

ABSTRACT WORD COUNT: 66

NOTE:

Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200017	480
CLAIMS B	(German)	200017	499
CLAIMS B	(French)	200017	604
SPEC B	(English)	200017	12384
Total word count - document A			0
Total word count - document B			13967
Total word count - documents A + B			13967

...SPECIFICATION Department of Computer Science, University of Essex,
Wivenhoe Park, Colchester, Essex, U.K. (1987) discloses such a system.

In Colley, the window modules are provided **by dividing** a display
memory into physically separate window areas. **Each** image signal window
is maintained in its entirety in a respective window module; the
visibility of overlapping portions of the windows is determined via
arbitration...

12/3,K/8 (Item 8 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00489888

Multimedia system

Multimediansystem

Systeme multimedia

PATENT ASSIGNEE:

International Business Machines Corporation, (200120), Old Orchard Road,
Armonk, N.Y. 10504, (US), (Proprietor designated states: all)

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LEGAL REPRESENTATIVE:

Burt, Roger James, Dr. (52152), IBM United Kingdom Limited Intellectual
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PATENT (CC, No, Kind, Date): EP 492795 A2 920701 (Basic)
EP 492795 A3 921230
EP 492795 B1 950920
EP 492795 B2 000426

APPLICATION (CC, No, Date): EP 91310692 911120;

PRIORITY (CC, No, Date): US 625564 901211

DESIGNATED STATES: DE; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-003/14; G09G-005/00

ABSTRACT WORD COUNT: 101

NOTE:

Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200017	414
CLAIMS B	(German)	200017	408
CLAIMS B	(French)	200017	484
SPEC B	(English)	200017	12373
Total word count - document A			0
Total word count - document B			13679
Total word count - documents A + B			13679

...SPECIFICATION Department of Computer Science, University of Essex,
Wivenhoe Park, Colchester, Essex, U.K. (1987) discloses such a system.

In Colley, the window modules are provided **by dividing** a display
memory into physically separate window areas. **Each** image signal window
is maintained in its entirety in a respective window module; the
visibility of overlapping portions of the windows is determined via
arbitration...

12/3,K/9 (Item 9 from file: 348)

DIALOG(R)File 348:EUROPEAN PATENTS

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00483660

Memory access bus arrangement

Busanordnung fur Speicherzugriff

Dispositif de bus d'accès a memoire

PATENT ASSIGNEE:

AT&T Corp., (589370), 32 Avenue of the Americas, New York, NY 10013-2412,
(US), (applicant designated states: DE;ES;FR;GB;IT)

INVENTOR:

Laha, Subhasis, 4320 Nutmeg Lane, Apt. 230, Lisle, Illinois 60532, (US)

Thompson, Dennis Joseph, 1815 Allen Drive, Geneva, Illinois 60134, (US)

LEGAL REPRESENTATIVE:

Buckley, Christopher Simon Thirsk et al (28912), Lucent Technologies (UK)
Ltd, 5 Mornington Road, Woodford Green, Essex IG8 0TU, (GB)

PATENT (CC, No, Kind, Date): EP 458516 A2 911127 (Basic)
EP 458516 A3 920408
EP 458516 B1 971105

APPLICATION (CC, No, Date): EP 91304338 910515;

PRIORITY (CC, No, Date): US 529051 900525

DESIGNATED STATES: DE; ES; FR; GB; IT

INTERNATIONAL PATENT CLASS: G06F-013/16;

ABSTRACT WORD COUNT: 180

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9710W5	1363
CLAIMS B	(German)	9710W5	1287
CLAIMS B	(French)	9710W5	1486

SPEC B (English) 9710W5 4279
Total word count - document A 0
Total word count - document B 8415
Total word count - documents A + B 8415

...SPECIFICATION wherein a processor accesses a bus at one interval and reserves an access on that bus during a second interval for the response from a **memory controller**. Both the **split** transaction arrangement and the pipeline **bus** are considerably more expensive than a tenured bus and continue to have substantial limitations on the total throughput of the bus thus creating a bottleneck...

12/3,K/10 (Item 10 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2003 European Patent Office. All rts. reserv.

00268199

Method and apparatus for sharing information between a plurality of processing units.

Verfahren und Vorrichtung zur gemeinsamen Informationsbenutzung zwischen einer Mehrzahl von Verarbeitungseinheiten.

Methode et appareil de partage d'information entre plusieurs unites de traitement.

PATENT ASSIGNEE:

ENCORE COMPUTER CORPORATION, (1194970), 257 Cedar Hill Street,
Marlborough, Massachusetts 01752-3089, (US), (applicant designated
states: DE;FR;GB)

INVENTOR:

Sood, Pardeep K., 8210 NW 8th Place, Plantation Florida 33324, (US)

Smith, Roger A., 1611 NW 63rd Avenue, Sunrise Florida 33313, (US)

Heeter, Timothy J., 2443 Tortugas Lane, Fort Lauderdale Florida 33312,
(US)

Roganti, Adriano, 5320 NW 31st Street, Margate Florida 33063, (US)

Acton, John D., 2200 SW 92nd Terrace, No. 2804, Fort Lauderdale Florida
33324, (US)

LEGAL REPRESENTATIVE:

Crawford, Andrew Birkby et al (29761), A.A. THORNTON & CO. Northumberland
House 303-306 High Holborn, London WC1V 7LE, (GB)

PATENT (CC, No, Kind, Date): EP 251686 A2 880107 (Basic)
EP 251686 A3 900530
EP 251686 B1 940119

APPLICATION (CC, No, Date): EP 87305634 870624;

PRIORITY (CC, No, Date): US 880222 860630

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-015/16;

ABSTRACT WORD COUNT: 80

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	563
CLAIMS B	(German)	EPBBF1	492
CLAIMS B	(French)	EPBBF1	625
SPEC B	(English)	EPBBF1	6252
Total word count - document A			0
Total word count - document B			7932
Total word count - documents A + B			7932

...SPECIFICATION to a reflective memory bus receive latch 150 connected thereto. The data is held within the latch 150 which is selectively enabled by the reflective **memory** bus control **logic** to receive data from the reflective memory bus transceivers except when a particular write sense controller is itself transmitting.

The information word taken from the...

...bus 156 to an upper link address comparator 158 and a lower link address comparator 160 for the purpose of determining whether the local shared

memory partition encompasses the address so supplied by the addition logic. The local **partition** is **defined** by information **supplied from** the address decode jumpers 92 to the second control register latch 90 which is connected via a bus 162 to the upper link address comparators...

...are instances, however, when different bounds may be desirable to be used. Thus, separate comparator circuitry has been provided to detect when the information received **from** the reflective memory **bus is within** the receive shared **partition**.

In the event that the information is within the address limits of the shared partition, enabling signals are supplied to a pair of leads 164...

12/3,K/11 (Item 11 from file: 348)
DIALOG(R) File 348:EUROPEAN PATENTS
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00262186

Debugging microprocessor.

Fehlersuchmikroprozessor.

Microprocesseur de deverminage.

PATENT ASSIGNEE:

NEC CORPORATION, (236690), 7-1, Shiba 5-chome Minato-ku, Tokyo 108-01,
(JP), (applicant designated states: DE;FR;GB)

INVENTOR:

Shouda, Masahiro c/o NEC Corporation, 33-1, Shiba 5-chome, Minato-ku
Tokyo, (JP)

LEGAL REPRESENTATIVE:

Glawe, Delfs, Moll & Partner Patentanwalte (100692), Postfach 26 01 62
Liebherrstrasse 20, W-8000 Munchen 26, (DE)

PATENT (CC, No, Kind, Date): EP 265949 A2 880504 (Basic)
EP 265949 A3 891025
EP 265949 B1 930324

APPLICATION (CC, No, Date): EP 87115911 871029;

PRIORITY (CC, No, Date): JP 86258915 861029

DESIGNATED STATES: DE; FR; GB

INTERNATIONAL PATENT CLASS: G06F-011/00; G06F-009/46;

ABSTRACT WORD COUNT: 114

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	533
CLAIMS B	(German)	EPBBF1	464
CLAIMS B	(French)	EPBBF1	662
SPEC B	(English)	EPBBF1	3271
Total word count - document A			0
Total word count - document B			4930
Total word count - documents A + B			4930

...CLAIMS interrupt (80) has been requested.

3. A debugging microprocessor claimed in Claim 2 wherein when the instruction execution unit (20) is notified that the non- **maskable** interrupt (30) has been requested, the instruction execution unit (20) reads the content of **a memory** location storing **a** branch destination address for a non-maskable interrupt operation, and when the instruction execution unit (20) is thereafter immediately notified that the debug interrupt (80...

...and the program status word, and then, moves to the operation of the debug interrupt.

4. A microprocessor development support system coupled with a first **memory** (58) **storing** a program to be debugged and receiving a non-maskable interrupt (30) from an external, comprising a controller (46) coupled to the first memory (58...

...word information, and the debugging microprocessor of any of claims 1 to 3 selectively coupled to one of said first memory (50) and said

second **memory** (62) so as to execute either the program to be debugged or the debugging program, said debugging microprocessor receiving said non-maskable interrupt (30) and said debug interrupt (80...

12/3,K/13 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00512761

INCREASING THE MEMORY PERFORMANCE OF FLASH MEMORY DEVICES BY WRITING
SECTORS SIMULTANEOUSLY TO MULTIPLE FLASH MEMORY DEVICES
AMELIORATION DE LA VITESSE DE LA MEMOIRE DANS UN DISPOSITIF A MEMOIRE FLASH
AU MOYEN D'UNE OPERATION D'ENREGISTREMENT EXECUTEE SIMULTANEMENT SUR
DES DISPOSITIFS MULTIPLES

Patent Applicant/Assignee:

LEXAR MEDIA INC,
ESTAKHRI Petro,
IMAN Berhanu,

Inventor(s):

ESTAKHRI Petro,
IMAN Berhanu,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9944113 A2 19990902

Application: WO 99US4247 19990225 (PCT/WO US9904247)

Priority Application: US 9830697 19980225

Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES

FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD

MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US

UZ VN YU ZW GH GM KE LS MW SD SL SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT

BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA

GN GW ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 16151

Fulltext Availability:

Claims

Claim

... for storing odd data bytes of said even sector, and
a second odd sector field for storing odd data bytes of said odd sector;
said **memory** bus includes,
a first **split** bus coupled to transmit said even data bytes of said
sectors between said memory
controller and said first **memory** unit;
a second **split** bus coupled to transmit said odd data bytes of said
sectors between said memory controller and said second memory unit.

4 A memory storage device as...of a
second sector;

said memory bus includes,

a first split bus coupled to transmit (least significant ?) data bytes of
said sectors between said

memory **controller** and said first **memory** unit;

a second **split** bus coupled to transmit (most significant ?) data
bytes of said sectors between said memory controller and said second
memory unit.

13 A memory storage device as...

12/3,K/14 (Item 3 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00422176 **Image available**

DYNAMIC SPARE COLUMN REPLACEMENT MEMORY SYSTEM

SYSTEME DYNAMIQUE DE MEMOIRE DE REMPLACEMENT A COLONNES DE RESERVE

Patent Applicant/Assignee:

I-CUBE INC,

Inventor(s):

WU Chun-Chu Archie,

WONG Chun-Chiu Daniel,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9812637 A1 19980326

Application: WO 97US17186 19970919 (PCT/WO US9717186)

Priority Application: US 96710571 19960919

Designated States: JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

Publication Language: English

Fulltext Word Count: 5598

Fulltext Availability:

Detailed Description

Detailed Description

... access. Referring to FIGS. 1 and 6, when

DRAM controller 20 receives a DRAM address on the ADDR bus along with control signals indicating a **memory** read cycle, **controller** 20 **breaks** the **bus** address into two parts, a "row address" and a "column address". Controller 20 initially (at time T0) places the row address on a set of...

12/3,K/15 (Item 4 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00353664 **Image available**

MULTIPLE SEQUENCE MPEG DECODER AND PROCESS FOR CONTROLLING SAME

DECODEUR MPEG A SEQUENCE MULTIPLE ET PROCESSUS DE COMMANDE

Patent Applicant/Assignee:

THE 3DO COMPANY,

Inventor(s):

WASSERMAN Steve C,

BALDWIN James Armand,

MITSUOKA George,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9636178 A1 19961114

Application: WO 96US6510 19960508 (PCT/WO US9606510)

Priority Application: US 95439085 19950510; US 95440464 19950510

Designated States: AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB

GE HU IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL

PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AM AZ

BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

BF BJ CF CG CI CM GA GN ML MR NE SN TD TG

Publication Language: English

Fulltext Word Count: 18262

Fulltext Availability:

Claims

Claim

... the motion video output

it DMA controller.

65. An MPEG decoding system, comprising:

a host system including a host system memory, a host system memory **controller**, a host system processor and a host system **bus**, the host system **memory** being **divided** into at least a storage area buffer, a first and a second display buffer buffers, a coded data

12/3,K/16 (Item 5 from file: 349)

DIALOG(R)File 349:PCT FULLTEXT

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00348329 **Image available**

BUS STRUCTURE FOR A MULTIPROCESSOR SYSTEM
STRUCTURE DE BUS POUR UN SYSTEME MULTIPROCESSEUR

Patent Applicant/Assignee:

INTERNATIONAL BUSINESS MACHINES CORPORATION,
GETZLAFF Klaus-Jorg,
WILLE Udo,
TAST Hans-Werner,
LEPPLA Bernd,

Inventor(s):

GETZLAFF Klaus-Jorg,
WILLE Udo,
TAST Hans-Werner,
LEPPLA Bernd,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9630842 A1 19961003

Application: WO 95EP1140 19950327 (PCT/WO EP9501140)

Priority Application: WO 95EP1140 19950327

Designated States: JP US AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

Publication Language: English

Fulltext Word Count: 6649

Fulltext Availability:

Detailed Description

Detailed Description

... according to the invention. The multiprocessor system exemplary consists of four processors 1, 2, 3, 4 with no private L2 cache memories and a main **memory** which is **divided** exemplary into a first **memory** bank built ...6 and a second memory bank built by two memory modules 7, 8. The memory banks 51 6 and 7, 8 are controlled by storage **controllers** (STCs) 9, 10.

The common **bus** system is **divided** in two logical busses 11, 12 which are labeled by logical reference numbers 0 and 1, respectively, wherein each of the logical busses comprises a...

12/3,K/17 (Item 6 from file: 349)

DIALOG(R) File 349: PCT FULLTEXT

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00332973 **Image available**

MONOLITHIC PC AUDIO CIRCUIT
CIRCUIT AUDIO MONOLITHIQUE POUR PC

Patent Applicant/Assignee:

ADVANCED MICRO DEVICES INC,

Inventor(s):

HEWITT Larry D,
BLUMENTHAL Jeffrey M,
BREHMER Geoffrey E,
BROWN Glen W,
CABLER Carlin Dru,
FEEMSTER Ryan,
GUERCIO David,
GULICK Dale E,
HOGAN Michael,
LINZ Alfredo R,
NORRIS David,
SCHNIZLEIN Paul G,
SOQUES Martin P,
SPAK Michael E,
SUGGS David N,
TOROK Alan T,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9615484 A2 19960523
Application: WO 95US14254 19951102 (PCT/WO US9514254)
Priority Application: US 94333386 19941102; US 94333451 19941102; US
94333460 19941102; US 94333467 19941102; US 94333536 19941102; US
94333564 19941102; US 94334461 19941102; US 94334462 19941102; US
95510139 19950803
Designated States: JP KR AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 98704

Fulltext Availability:
Detailed Description

Detailed Description

... is implemented in the same way as that used by the PC Net ISA chip,
79C960/1. The third design aspect is that the data bus is
broken up into a few groups, each of which is skewed from the others,
as
shown in the Fig. 14a.
3. Register Data Bus I/O...indicates the circuit C
is in shut-down mode, initiated by a specific I/O write to PPWRL
The 2XX and 3XX decodes are further broken down as follows.

TABLE X
SAM01 2XX signal Faibles
0h IDEC2X0
6h IDEC2X6
8h MEC2X8 IDECI[01
9h IDEC2X9 IDECI[01
Ah MEC2XA I]DECI...mode.

The 100 microsecond timers referenced in Fig. 26 consist of two
conventional timer circuits within logic block 158 (Fig. 12), each driven
by ICLK100K (divide by 10). One of the timers is used to count out the
goingto-low-power-state time and the other is used to count out...

12/3,K/18 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00224793

CACHE SUBSYSTEM FOR MICROPROCESSOR BASED COMPUTER WITH ASYNCHRONOUS AND
SYNCHRONOUS DATA PATH
SOUS-SYSTEME D'ANTEMEMOIRE POUR ORDINATEUR A MICROPROCESSEUR A VOIE DE
DONNEES SYNCHRONE ET ASYNCHRONE

Patent Applicant/Assignee:

INTEL CORPORATION,
Inventor(s):
MACWILLIAMS Peter D,
WEBB Clair C,
FARRELL Robert L,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9222035 A1 19921210
Application: WO 92US4744 19920604 (PCT/WO US9204744)
Priority Application: US 9179 19910604
Designated States: AT BE CH DE DE DK ES FR GB GB GR IT JP LU MC NL SE
Publication Language: English
Fulltext Word Count: 17219

Fulltext Availability:
Detailed Description

Detailed Description

... operate
asynchronously on the CPU bus and memory bus interfaces, there
are no synchronizers internal to this device. Synchronizers for data
transfer reside within the memory bus controller I 1 partition .

The byte enable latch 18 is properly associated with the cache controller partition in Figure 1. The byte enable latch provides an interface for isolated...

12/3,K/19 (Item 8 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00224789

INTEGRATED CACHE SRAM

MEMOIRE RAM STATIQUE D'ANTEMEMOIRE INTEGREE

Patent Applicant/Assignee:

INTEL CORPORATION,

Inventor(s):

MacWILLIAMS Peter D,

WEBB Clair C,

FARRELL Robert L,

Patent and Priority Information (Country, Number, Date):

Patent: WO 9222031 A1 19921210

Application: WO 92US4747 19920604 (PCT/WO US9204747)

Priority Application: US 9175 19910604

Designated States: AT BE CH DE DE DK ES FR GB GB GR IT JP LU MC NL SE

Publication Language: English

Fulltext Word Count: 16783

Fulltext Availability:

Detailed Description

Detailed Description

... operate

asynchronously on the CPU bus and memory bus interfaces, there are no synchronizers internal to this device. Synchronizers for data transfer reside within the **memory bus controller 11 partition**.

The byte enable latch 18 is properly associated with the cache controller partition in Figure 1. The byte enable latch provides an interface for isolated...

10/5/1 (Item 1 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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06285148 E.I. No: EIP03057345621

Title: System-level design of IEEE 1394 bus segment bridge

Author: Yamamoto, Hirofumi; Chikamura, Keishi; Shigiya, Atsuhito; Tsujino, Kosuke; Izumi, Tomonori; Onoye, Takao; Nakamura, Yukihiro

Corporate Source: Dept. of Communications Engineering Kyoto University, Kyoto 606-8501, Japan

Conference Title: 15th International Symposium on System Synthesis

Conference Location: Kyoto, Japan Conference Date: 20021002-20021004

Sponsor: ACM SIGDA; IEEE Computer Society

E.I. Conference No.: 60631

Source: Proceedings of the International Symposium on System Synthesis 2002. p 74-79 (IEEE cat n 02EX631)

Publication Year: 2002

CODEN: PISSFW ISSN: 1080-1820

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical); X; (Experimental)

Journal Announcement: 0302W1

Abstract: A system simulation environment is constructed dedicatedly for IEEE1394 high-speed digital communication. In this environment, various network transactions inherent in communication systems are taken into account for system simulation, which is indispensable to enable IP (Intellectual Property)-based design of the systems. By using the proposed environment, system-level design of IEEE1394 link layer **controller** and **bus segment** bridge is achieved with great ability of network transactions as well as connectivities with physical layer chips. Functionalities of the designed bus segment bridge has been verified according to its FPGA implementation. 11 Refs.

Descriptors: *Digital communication systems; Computer aided design; Field programmable gate arrays; Logic design; Logic programming; Computer simulation languages; C (programming language)

Identifiers: Bus segment bridge; System simulation; High speed digital communication; Intellectual property design

Classification Codes:

723.1.1 (Computer Programming Languages)

722.3 (Data Communication, Equipment & Techniques); 723.5 (Computer Applications); 721.2 (Logic Elements); 723.1 (Computer Programming)

722 (Computer Hardware); 723 (Computer Software, Data Handling & Applications); 721 (Computer Circuits & Logic Elements)

72 (COMPUTERS & DATA PROCESSING)

10/5/2 (Item 2 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

05942251 E.I. No: EIP01476734904

Title: A 1GHz power efficient single chip multiprocessor system for broadband networking applications

Author: Santhanam, S.; Allmon, R.; Anne, K.; Blake, R.; Bunker, N.; Campbell, B.; Carlson, M.; Chen, Z.; Cheng, J.; Do, T.; Dobberpuhl, D.; Ingino, J.; Kidd, D.; Kruckemyer, D.; Lee, J.; et al.

Corporate Source: Broadcom Corporation, San Jose, CA, United States

Conference Title: 2001 VLSI Circuits Symposium

Conference Location: Kyoto, Japan Conference Date: 20010614-20010616

Sponsor: Japan Society of Applied Physics; IEEE

E.I. Conference No.: 58690

Source: IEEE Symposium on VLSI Circuits, Digest of Technical Papers n CIRCUITS SYMP. 2001. p 107-110 (IEEE cat n 01CH37185)

Publication Year: 2001

CODEN: 85PXA5

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 0111W4

Abstract: The Broadcom BCM12500 is a high performance system on a chip (SOC) targeted at network centric tasks. The chip consists of two high performance SB-1 MIPS64 trademark CPU's, a shared 512KB L2 cache, a **DDR memory controller**, and integrated I/O. All major blocks of the processor are connected together via the ZBbus trademark a high speed **split transaction fully coherent multi processor bus**. Three Gigabit Ethernet MAC's enable a direct interface to network elements. High-speed system I/O is provided using AMD's Lightning Data Transport (LDT trademark) I/O fabric and a 66MHz PCI bus. The die measures 14.2mm by 13.3mm in a bulk 0.15um CMOS technology and has a power dissipation of 13W at 1.2V and 1GHz. 4 Refs.

Descriptors: *Microprocessor chips; Broadband networks; CMOS integrated circuits; Energy dissipation; Static random access storage

Identifiers: Lightning data transport (LDT)

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits); 525.4 (Energy Losses/Dissipation)

714 (Electronic Components & Tubes); 721 (Computer Circuits & Logic Elements); 716 (Electronic Equipment, Radar, Radio & Television); 525 (Energy Management)

71 (ELECTRONICS & COMMUNICATION ENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 52 (FUEL TECHNOLOGY)

10/5/3 (Item 3 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

(c) 2003 Elsevier Eng. Info. Inc. All rts. reserv.

05550398 E.I. No: EIP00055160141

Title: Single-chip, 1.6-billion, 16-b MAC/s multiprocessor DSP

Author: Ackland, B.; Anesko, A.; Brinthaup, D.; Daubert, S.J.; Kalavade, A.; Knobloch, J.; Micca, E.; Moturi, M.; Nicol, C.J.; O'Neill, J.H.; Othmer, J.; Sackinger, E.; Singh, K.J.; Sweet, J.; Terman, C.J.; et al

Corporate Source: Lucent Technologies, Holmdel, NJ, USA

Source: IEEE Journal of Solid-State Circuits v 35 n 3 2000. p 412-424

Publication Year: 2000

CODEN: IJSCBC **ISSN:** 0018-9200

Language: English

Document Type: JA; (Journal Article) **Treatment:** T; (Theoretical)

Journal Announcement: 0006W4

Abstract: An MIMD multiprocessor digital signal- processing (DSP) chip containing four 64-b processing elements (PE's) interconnected by a 128-h pipelined **split transaction bus** (STBus) is presented. Each PE contains a 32-b RISC core with DSP enhancements and a 64-b single-instruction, multiple-data vector coprocessor with four 16-b MAC/s and a vector reduction unit. PE's are connected to the STBus through reconfigurable dual-ported snooping L1 cache memories that support shared memory multiprocessing using a modified-MESI data coherency protocol. High-bandwidth data transfers between system memory and on-chip caches are managed in a pipelined **memory controller** that supports multiple outstanding transactions. An embedded RTOS dynamically schedules multiple tasks onto the PE's. Process synchronization is achieved using cached semaphores. The 200-mm*2, 0.25- mu m CMOS chip operates at 100 MHz and dissipates 4 W from a 3.3-V supply. (Author abstract) 12 Refs.

Descriptors: *Digital signal processing; Pipeline processing systems; Microprocessor chips; Interconnection networks; Buffer storage; Network protocols; Embedded systems; CMOS integrated circuits

Identifiers: Pipelined **split transaction bus** (STBus); Data coherency protocols

Classification Codes:

722.4 (Digital Computers & Systems); 703.1 (Electric Networks); 722.1 (Data Storage, Equipment & Techniques); 714.2 (Semiconductor Devices & Integrated Circuits)

722 (Computer Hardware); 703 (Electric Circuits); 723 (Computer Software); 714 (Electronic Components)

72 (COMPUTERS & DATA PROCESSING); 70 (ELECTRICAL ENGINEERING); 71 (ELECTRONICS & COMMUNICATIONS)

10/5/4 (Item 4 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
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03911872 E.I. No: EIP94081359298

Title: High speed optical bus network system consisting of optical fiber and star coupler

Author: Suzuki, M.; Hamazaki, Y.; Sakamoto, K.; Tsukamoto, M.; Okada, Y.
Source: Denshi Gijutsu Sogo Kenkyusho Iho/Bulletin of the
Electrotechnical Laboratory v 58 n 1 1994. p 27-38
Publication Year: 1994
CODEN: DGSKAR ISSN: 0366-9092
Language: English; Japanese
Document Type: JA; (Journal Article) Treatment: A; (Applications); G;
(General Review)
Journal Announcement: 9409W4

Abstract: A high-speed optical communication system, called 'optical bus' is described. The optical bus is a token-passing bus network consisting of an optical transmission medium (composed of an optical star coupler and optical fibers) and optical bus interfaces. The optical bus interface could be divided into two parts, an optical bus controller and a dual-port memory (DPM) controller. The optical bus controller is hard-wired high-speed logic circuits which performs basic operations, i.e. token passing, packet transmission and reception. On the other hand, the DPM controller is a programmable controller which performs complex operation like logical-ring reconstruction, and provides DPM view of interface to host processor. The optical bus is designed to connect limited number of processors, up to several tens of them, on a floor. Simple transmission medium and its limited propagation delay, high-performance optical bus controller and intelligent DPM controller make the optical bus high data transfer rate and low latency computer network. The developed prototype system achieves 400 Mbps of data transfer rate and 900 ns of token relay time. (Translated author abstract) 10 Refs.

Descriptors: *Optical communication equipment; Data communication systems ; Optical fiber coupling; Interfaces (computer); Logic circuits; Program processors; Programmed control systems; Computer networks; Fiber optics

Identifiers: Optical bus network system; Optical transmission medium; Optical star coupler; Optical bus interface; Optical bus controller; Dual port memory controller ; Data transfer rates; Token relay time

Classification Codes:
741.1.2 (Fiber Optics)
717.1 (Optical Communication Systems); 717.2 (Optical Communication Equipment); 722.3 (Data Communication, Equipment & Techniques); 741.1 (Light/Optics); 721.3 (Computer Circuits); 721.2 (Logic Elements)
717 (Electro-Optical Communications); 722 (Computer Hardware); 741 (Optics & Optical Devices); 721 (Computer Circuits & Logic Elements)
71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 74 (OPTICAL TECHNOLOGY)

10/5/5 (Item 5 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
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03013344 E.I. Monthly No: EIM9101-003344

Title: ECL RISC microprocessor designed for two level cache.

Author: Roberts, David; Layman, Tim; Taylor, George
Corporate Source: MIPS Computer Systems, Inc, Sunnyvale, CA, USA
Conference Title: Digest of Papers - Thirty-Fifth IEEE Computer Society International Conference - COMPCON Spring '90
Conference Date: 19900226
Sponsor: IEEE Computer Soc
E.I. Conference No.: 13939
Source: Dig of Pap Thirty Fifth IEEE Comput Soc Int Conf COMPCON 89. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2843-1). p 228-231

Publication Year: 1990
ISBN: 0-8186-2028-5
Language: English
Document Type: PA; (Conference Paper) Treatment: T; (Theoretical); A;
(Applications)
Journal Announcement: 9101

Abstract: Reduced-instruction-set-computer (RISC) architectures, by virtue of their streamlined instruction set and more efficient use of fundamental machine resources, are capable of exploiting emerging VLSI technologies more quickly than traditional, more complicated machine architectures. Bipolar emitter-coupled-logic (ECL) technology offers shorter propagation delays and higher toggle rates than other circuit technologies. This, coupled with its ability to drive transmission lines and large capacitive loads, has made ECL the technology of choice for many high-speed computer systems. The lower circuit density and high-power requirements of traditional ECL have prevented its use in low-cost microprocessor-based system designs. Recent advances in density and power consumption of VLSI ECL technology have widened the technology envelope to the point at which it has become an attractive target for RISC processor designs. The four VLSI chips described provide address translation, the control logic for a two-level cache, and a system bus interface in addition to the basic integer and floating-point data paths. The chip set consists of the R6000 CPU, the R6010 floating-point **controller**, the BIT B3110 floating-point multiply/divide unit, and the R6020 system **bus controller**. 7 Refs.

Descriptors: *COMPUTER ARCHITECTURE--*Reduced Instruction Set Computing; LOGIC CIRCUITS, EMITTER COUPLED; INTEGRATED CIRCUITS, VLSI

Identifiers: TWO-LEVEL CACHE; RISC MICROPROCESSOR; STREAMLINED INSTRUCTION; TOGGLE RATES; VLSI ECL; HIGH-SPEED COMPUTER

Classification Codes:

722 (Computer Hardware); 723 (Computer Software); 721 (Computer Circuits & Logic Elements); 713 (Electronic Circuits); 714 (Electronic Components)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

10/5/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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01644227 E.I. Monthly No: EIM8404-029156
Title: OMEGA IMPROVES PRODUCTIVITY 50%.
Author: La Cagnina, Michael L.
Corporate Source: Westinghouse Electric Corp
Conference Title: 20th Annual Conference - National Council of Physical Distribution Management.
Conference Location: San Francisco, Calif, USA Conference Date: 19821010
Sponsor: Natl Council of Physical Distribution Management, Oak Brook, Ill, USA
E.I. Conference No.: 03780
Source: v 1. Publ by Natl Council of Physical Distribution Management, Oak Brook, Ill, USA p 293-314
Publication Year: 1982
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8404
Descriptors: *MARKETING
Identifiers: DISTRIBUTION FACILITY LOCATION STUDY; MOTOR **CONTROLLERS** ; PUSH-BUTTONS; CIRCUIT **BREAKERS** ; CIRCUIT DEVICES; **BUS** DUCT; FLOW-RACK AREA; PALLET RACK AREA; STRADDLE-REACH TRUCK ACCESS; INVENTORY ASSIGNMENT; DISTRIBUTION OPERATION COMPUTERIZATION
Classification Codes:
911 (Industrial Economics)
91 (ENGINEERING MANAGEMENT)

10/5/7 (Item 7 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)
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00777404 E.I. Monthly No: EI7805034572

Title: DETECTING ELECTRICAL POWER SYSTEM PROBLEMS BY INFRARED SURVEY.

Author: Galto, Edward J.

Corporate Source: Norwich Pharm Co, NY

Source: Plant Engineering (Barrington, Illinois) v 31 n 26 Dec 22 1977 p 71-74

Publication Year: 1977

CODEN: PLENAB ISSN: 0032-082X

Language: ENGLISH

Journal Announcement: 7805

Abstract: The New Brunswick, NJ, plant of E. R. Squibb & Sons, Inc. , conducted an infrared survey of the electric power system to detect incipient problems. Survey work was contracted to an electrical apparatus service company. The agreement called for testing high-voltage fuse connections, knife switches, disconnect and transfer switches, terminations, and transformers. Low-voltage equipment that was checked included bus bar connections, breakers , stab connections, wire terminals, power panels, lighting panels, and motor controllers . More than 5000 potential trouble spots were investigated in the course of the 5-day survey. An infrared survey was conducted to detect and analyze overloaded components and poor connections. An overload or a poor connection will cause overheating, which can be detected as infrared radiation. Infrared detection permits inspection of far more points in far less time than any other technique for checking for electrical overloads or electrical connection integrity. The only requirements for conducting an infrared survey are that the points to be checked must be operating under load and accessible to the scanner. Entire panels and enclosures can be scanned with the covers intact. If an unusual amount of heat is detected, the covers can be removed and another scan made to pinpoint which component is responsible for the heat. No service interruption is required for the survey. The most common causes of problems detected by the survey were knife-blade and cartridge-type fuse clips. Loose bolted connections were also a common cause of heat buildup, especially in high-vibration areas. Several cases of overloading and load imbalance were also detected, including a phase imbalance condition that would probably have caused motor failure.

Descriptors: *INDUSTRIAL PLANTS--*Fault Location; INFRARED IMAGING--Applications

Classification Codes:

402 (Buildings & Towers); 706 (Electric Transmission & Distribution); 942 (Electrical & Electronic Measuring Instruments); 741 (Optics & Optical Devices)

40 (CIVIL ENGINEERING); 70 (ELECTRICAL ENGINEERING); 94 (INSTRUMENTS & MEASUREMENT); 74 (OPTICAL TECHNOLOGY)

10/5/8 (Item 1 from file: 2)

DIALOG(R) File 2: INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

03885643 INSPEC Abstract Number: C91036455

Title: Virtual memory techniques using the VL86C110 memory controller

Author(s): Cates, R.; Farrell, J.J., II

Author Affiliation: VLSI Technol. Inc., Tempe, AZ, USA

Conference Title: Wescon/88 Conference Record p.5.3/1-6

Publisher: Electron. Conventions Manage, Ventura, CA, USA

Publication Date: 1988 Country of Publication: USA 798 pp.

Conference Sponsor: IEEE; ERA

Conference Date: 15-17 Nov. 1988 Conference Location: Anaheim, CA, USA

Language: English Document Type: Conference Paper (PA)

Abstract: Examines the memory management considerations and aspects of a high-performance RISC-based microprocessor system. System implementations, including bank switching, paging, segmentation, partitioning , bus structure and virtual address translation are discussed. (1 Refs)

Subfile: C

Descriptors: storage management chips; virtual machines
Identifiers: VL86C110 **memory controller** ; memory management;
RISC-based microprocessor system; bank switching; paging; segmentation;
partitioning; bus structure; virtual address translation
Class Codes: C6120 (File organisation); C5150 (Other circuits for
digital computers); C5380 (Other aspects of storage devices and techniques
)

10/5/9 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2003 Institution of Electrical Engineers. All rts. reserv.

02125339 INSPEC Abstract Number: B83056185, C83038822
Title: Local area networks-high speed networks for office communications
Author(s): Fromm, I.
Author Affiliation: Siemens AG, Munchen, West Germany
Journal: Bulletin de l'Association Suisse des Electriciens (Organe Commun
de l'Association Suisse des Electriciens (ASE) et de l'Union des Centrales
Suisses d'Electricite (UCS)) vol.74, no.11 p.585-9
Publication Date: 4 June 1983 Country of Publication: Switzerland
CODEN: BUSEAH ISSN: 0036-1321
Language: German Document Type: Journal Paper (JP)
Treatment: General, Review (G)
Abstract: Local area networks allow data transmission between station
over distances from about 100 m to a few km, with data rate between 10
kbit/s and 20 Mbit/s. Using line, coaxial, or optical fibre cables, network
configurations can be mixed, star, ring or bus connected, with remote or
central control using a variety of access methods. Ring and bus networks
are described. The ring network using token access suffers from
disadvantages that one station malfunction affects the whole system, and
that steps must be taken to prevent effects of token corruption. Bus
connected networks use mostly matched coaxial cable as their transmission
medium, with CSMA/CD access. Carrier sense multiple access with collision
detection is briefly explained. Bus systems have advantages over ring
networks, but more recent broadband systems using frequency multiplexing
have difficulties in data collision avoidance management. Local area
network standardisation is discussed with reference to IEEE, ECMA, ISO, and
DIN considerations. The Siemens EMS bus network is introduced, being a
coaxial bus structure with 10 Mbit/s data rate, maximum distance between
two stations of 2.5 km, maximum number of connections 1024, serving several
bus segments via repeaters. Station transceiver and **controller**
functions, traffic behavioural aspects including channel utilization
related to data packet length and waiting times dependent on access method
and system loading, and practical utilization of bus network islands
interconnected by local branch exchanges are described. (7 Refs)

Subfile: B C
Descriptors: computer networks; office automation
Identifiers: local area networks; carrier sense multiple access; packet
switching; high speed networks; office communications; data transmission;
bus networks; ring network; token access; collision detection; Siemens EMS
bus network
Class Codes: B6210L (Computer communications); C5620 (Computer networks
and techniques); C7100 (Business and administration)

10/5/10 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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01831393 INSPEC Abstract Number: C82015127
Title: A vision system with splitting bus
Author(s): Dessimoz, J.-D.; Birk, J.; Kelley, R.; Hall, J.
Author Affiliation: Robot Res. Group, Univ. of Rhode Island, Kingston,
RI, USA
Conference Title: 1981 IEEE Computer Society Workshop on Computer
Architecture for Pattern Analysis and Image Database Management p.62-6
Publisher: IEEE, New York, NY, USA

Publication Date: 1981 Country of Publication: USA ix+348 pp.
Conference Date: 11-13 Nov. 1981 Conference Location: Hot Springs, VA,
USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: Describes a vision system which belongs to the MIMD class of multi-processor systems with reconfigurable architecture. Recursivity, pipeline mode, and parallelism are provided in order to cope with the bulk of information flowing from vision sensors. A single **bus**, **split** at picture frame rate by a programmable **controller**, allows simultaneous operation of several processors, while bus contention is kept to a minimum. System memories are time-shared, reducing necessary data transfers. Of interest also is the high degree of flexibility of the system, which can mix many types of processor/module under minimal constraints of: (1) bus-level hardware conventions and (2) frame rate synchronization. Uniformity in speed is not required among processors at high rate. Each can follow its own clock for picture element analysis, array processing, or any fast transaction. (21 Refs)

Subfile: C

Descriptors: computerised picture processing; multiprocessing systems

Identifiers: recursivity; vision system; splitting bus; MIMD;
multi-processor systems; pipeline mode; parallelism; vision sensors

Class Codes: C5220 (Computer architecture); C5260 (Digital signal
processing)

10/5/11 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-Eplus

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01230541 JICST ACCESSION NUMBER: 91A0080027 FILE SEGMENT: JICST-E
**Standard of remote-control systems for television production equipment (ES
bus).**

SHIMADA TETSUZO (1)

(1) NHK

Terebijon Gakkaishi(Journal of the Institute of Television Engineers of
Japan), 1990, VOL.44,NO.11, PAGE.1557-1560, FIG.5, TBL.2, REF.11

JOURNAL NUMBER: F0330ABG ISSN NO: 0386-6831

UNIVERSAL DECIMAL CLASSIFICATION: 621.397+654.197 621.39

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Commentary

MEDIA TYPE: Printed Publication

ABSTRACT: ES bus (EBU/SMPTE bus) which is the standard of remote control
of television production apparatus (VTR,ATR and telecine) was
introduced. ES bus construct LAN for communication with intelligent
interface tributer of each single apparatus mainly on **bus
controllers** . Each single apparatus is **divided** into controlling
equipment and controled equipment.

DESCRIPTORS: standard(specification); television broadcast; program
production; hierarchical structure; studio equipment; LAN; control
equipment; protocol; data bus; interconnection; VTR; telecine camera;
remote control

BROADER DESCRIPTORS: standard; broadcast; telecommunication; studio
technique; technology; structure; facility; computer network;
communication network; information network; network; equipment; rule;
bus(transmission line); transmission line; connection; magnetic tape
recorder; magnetic recorder; recording equipment; video recorder;
telecine apparatus; communication apparatus; control

CLASSIFICATION CODE(S): ND12031N; ND01000D

13/5/1 (Item 1 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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05686362 E.I. No: EIP00105377813

Title: New method for protection zone selection in microprocessor-based bus relays

Author: Qin, Bai-Lin; Guzman-Casillas, Armando; Schweitzer, Edmund O. III

Corporate Source: Schweitzer Engineering Lab, Inc, Pullman, WA, USA

Source: IEEE Transactions on Power Delivery v 15 n 3 Jul 2000. p 876-887

Publication Year: 2000

CODEN: ITPDE5 ISSN: 0885-8977

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical)

Journal Announcement: 0012W1

Abstract: Use of graph theory simplifies representation of complex bus arrangements in power system stations. This paper presents a new method, based upon graph theory, for selecting bus protection zones in microprocessor-based relays. We use a typical bus arrangement to illustrate the **graphical** representation of station arrangements, graph operations, and associated matrix operations. We also describe an implementation of the zone selection method and use two examples to demonstrate the advantages of the method. Using the status of switching devices in the station, the zone selection method provides the relay with real-time bus arrangement information. The bus relay uses this information to assign input currents to a differential protection zone and to select which **breakers** to trip for a **bus** fault or **breaker** failure. (Author abstract) 15 Refs.

Descriptors: *Relay protection; Busbars; Microprocessor chips; Matrix algebra; Graph theory; Electric fault location; Electric circuit breakers

Identifiers: Protective zone selections

Classification Codes:

914.1 (Accidents & Accident Prevention); 706.2 (Electric Power Lines & Equipment); 714.2 (Semiconductor Devices & Integrated Circuits); 921.1 (Algebra); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory)

706 (Electric Transmission & Distribution); 914 (Safety Engineering); 714 (Electronic Components); 921 (Applied Mathematics)

70 (ELECTRICAL ENGINEERING); 91 (ENGINEERING MANAGEMENT); 71 (ELECTRONICS & COMMUNICATIONS); 92 (ENGINEERING MATHEMATICS)

13/5/2 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)
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04622044 E.I. No: EIP97023517500

Title: Hardware-software cosynthesis for the Riley system

Author: Cheung, Peter Y.K.; Luk, Wayne; Mackinlay, Patrick I.

Corporate Source: Imperial Coll, London, UK

Conference Title: Proceedings of 1996 IEE Colloquium Hardware-Software Cosynthesis for Reconfigurable Systems

Conference Location: London, UK **Conference Date:** 19960222

E.I. Conference No.: 45940

Source: IEE Colloquium (Digest) n 036 1996. 5p

Publication Year: 1996

CODEN: DCILDN **ISSN:** 0963-3308

Language: English

Document Type: JA; (Journal Article) **Treatment:** G; (General Review)

Journal Announcement: 9704W1

Abstract: A cosynthesis and visualization system is described for the study of the interaction between hardware and software for a number of applications. Investigations of the use of different types of instructions of a processor when a pattern matching algorithm is executed, and the effect on the resource utilization, memory usage and **bus** traffic of different ways of **partitioning** functions on a JPEG **image** compression algorithm between software and hardware resources on the Riley board brought insights into the strength and limitations of the Riley system. A way of combining existing commercially available tools for VHDL synthesis

and simulation, conventional design descriptions with other new tools and languages in a coherent framework appeared promising. 4 Refs.

Descriptors: Computer architecture; Computer hardware; Computer software; Interfaces (computer); Microprocessor chips; Data storage equipment; **Image** compression; Algorithms; Software engineering; Computer hardware description languages

Identifiers: Hardware software cosynthesis; Riley system

Classification Codes:

722.2 (Computer Peripheral Equipment); 714.2 (Semiconductor Devices & Integrated Circuits); 722.1 (Data Storage, Equipment & Techniques)

722 (Computer Hardware); 723 (Computer Software); 714 (Electronic Components); 721 (Computer Circuits & Logic Elements)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

13/5/3 (Item 3 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

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03593688 E.I. Monthly No: EIM9304-024457

Title: **Algorithm for dynamic object tracking.**

Author: Datcu, Mihai P.; Folta, Florin; Toma, Cristian E.

Corporate Source: Polytechnic Inst. of Bucharest (Romania), Zurich, Switzerland

Conference Title: Intelligent Robots and Computer Vision XI: Algorithms, Techniques, and Active Vision

Conference Location: Boston, MA, USA Conference Date: 19921116

Sponsor: SPIE - Int Soc for Opt Engineering, Bellingham, WA, USA

E.I. Conference No.: 17849

Source: Proceedings of SPIE - The International Society for Optical Engineering v 1825. Publ by Int Soc for Optical Engineering, Bellingham, WA, USA. p 389-394

Publication Year: 1993

CODEN: PSISDG ISSN: 0277-786X ISBN: 0-8194-1026-8

Language: English

Document Type: PA; (Conference Paper) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 9304

Abstract: The purpose of this paper is to present a hierarchic processor architecture for the tracking of moving objects. Two goals are envisaged: the definition of a moving window for the target tracking, and multiresolution segmentation needed for scale independent target recognition. Memory windows in single processor systems obtained by software methods are limited in speed for high complexity **images**. In a multiprocessor system the limitation arises in bus or memory bottleneck. Highly concurrent system architectures have been studied and implemented as crossbar bus systems, multiple buses systems, or hypercube structures. Because of the complexity of these architectures and considering the particularities of **image** signals we suggest a hierarchic architecture that reduces the number of connections preserving the flexibility and which is well adapted for multiresolution algorithm implementations. The hierarchy is a quadtree. The solution is in using switched **bus** and block memory **partition** (granular **image** memory organization). 11 refs.

Descriptors: PATTERN RECOGNITION; TRACKING (POSITION); **IMAGE** ANALYSIS; HIERARCHICAL SYSTEMS; TREES (MATHEMATICS); COMPUTER ARCHITECTURE; FRACTALS

Identifiers: DYNAMIC OBJECT TRACKING; MOVING WINDOW; MULTIREOLUTION SEGMENTATION; SCENE ANALYSIS; TEXTURE ANALYSIS; FRACTAL TRANSFORM

Classification Codes:

723 (Computer Software); 921 (Applied Mathematics); 722 (Computer Hardware)

72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

13/5/4 (Item 4 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

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03513255 E.I. Monthly No: EIM9211-057133

Title: Signal processing, storage and display for towed array data.
Author: Craig, D. W.
Corporate Source: Defence Res Establ Pacific, Victoria, BC, Canada
Conference Title: Proceedings of Oceans '91
Conference Location: Honolulu, HI, USA **Conference Date:** 19911001
Sponsor: IEEE Oceanic Engineerig Soc
E.I. Conference No.: 16933
Source: Ocean Technologies and Opportunities in the Pacific for the 90's
 Proc Oceans 91 Oceans (New York) v 3. Publ by IEEE, IEEE Service Center,
 Piscataway, NJ, USA (IEEE cat n 91CH3063-5). p 1223-1228
Publication Year: 1991
CODEN: OCNSDK **ISSN:** 0197-7385
Language: English
Document Type: PA; (Conference Paper) **Treatment:** A; (Applications); T;
 (Theoretical)
Journal Announcement: 9211
Abstract: A novel signal processing and display system is being developed
 for the Canadian Ocean Acoustics Measurement System (COAMS), a towed
 hydrophone array 2 km in length. The main features of the system include
 simultaneous beamforming of data from four acoustic sub-apertures using
 multiple CPU/vector accelerators, online storage and recall of up to six
 gigabytes (GB) of normalized sonar **images**, and optical tape storage of up
 to 1 terabyte (1000 GB) of acoustic data. Other features include a PC-based
 array simulator, hardware time-domain interpolation beamformer, and a
 helical-scan recorder storing 4.5 GB of acoustic data on a VCR tape
 cartridge. An overview of the system is given, results are presented for
 system **bus** loading, and signal **partitioning** considerations are given
 for optimal real-time performance. 5 Refs.
Descriptors: *ACOUSTIC SIGNAL PROCESSING--*Marine Applications; ACOUSTIC
 VARIABLES MEASUREMENT--Marine Applications; ACOUSTIC VARIABLES MEASUREMENT
 --Acoustic Field
Identifiers: TOWED ARRAY DATA; BEAM FORMING; DATA DISPLAY; CANADA
Classification Codes:
 751 (Acoustics); 471 (Marine Science & Oceanography); 723 (Computer
 Software); 752 (Sound Equipment & Systems)
 75 (ACOUSTICAL TECHNOLOGY); 47 (OCEAN TECHNOLOGY); 72 (COMPUTERS &
 DATA PROCESSING)

13/5/5 **(Item 5 from file: 8)**
 DIALOG(R)File 8: Ei Compendex(R)
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03336756 E.I. Monthly No: EIM9111-057920
Title: A communication network for distributed database systems.
Author: Woo, Tai-Kuo
Corporate Source: Dept of Comput & Inf Sci, Jacksonville Univ, FL, USA
Conference Title: IEEE Proceedings of Southeastcon '90 - Technologies
 Today and Tomorrow
Conference Location: New Orleans, LA, USA **Conference Date:** 19900401
Sponsor: IEEE Region 3; South Central Bell; Northern Telecom Inc; AT&T
 Network Systems; Louisiana Power & Light Co; et al
E.I. Conference No.: 14990
Source: Conference Proceedings - IEEE SOUTHEASTCON v 3. Publ by IEEE,
 IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2883-7). p
 1021-1025
Publication Year: 1990
CODEN: CPISDM **ISSN:** 0734-7502
Language: English
Document Type: PA; (Conference Paper) **Treatment:** T; (Theoretical); A;
 (Applications)
Journal Announcement: 9111
Abstract: A graph traversal algorithm and its application to a
 dynamically **partitionable bus** network for a distributed database system
 are presented. The approach can be summarized as follows: (1) transform
 database operations into a graph where vertices represent database
 operations and edges denote the conflicts of using system resources among
 database operations, (2) color the constructed graph so that the vertices

corresponding to the nonconflicting database operations are assigned the same color, and (3) allow the nonconflicting database operations to proceed in parallel. The graph traversal algorithm used to color the vertices of a graph is described. The dynamic **bus partitioning** technique for a distributed database system is delineated. 10 Refs.

Descriptors: DATABASE SYSTEMS--*Management; COMPUTER PROGRAMMING--Algorithms; COLOR; COMPUTER **GRAPHICS** ; COMPUTER NETWORKS; **GRAPHIC METHODS**

Identifiers: GRAPH TRAVERSAL ALGORITHMS; DYNAMICALLY **PARTITIONABLE BUS NETWORKS**; DISTRIBUTED DATABASE SYSTEMS

Classification Codes:

723 (Computer Software); 902 (Engineering Graphics & Standards); 741 (Optics & Optical Devices)
72 (COMPUTERS & DATA PROCESSING); 90 (GENERAL ENGINEERING); 74 (OPTICAL TECHNOLOGY)

13/5/6 (Item 6 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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03029490 E.I. Monthly No: EI9103024951

Title: Flexibly Coupled Multiprocessors for image processing.

Author: Sunwoo, Myung Hoon; Aggarwal, J. K.

Corporate Source: Univ of Texas at Austin, Austin, TX, USA

Source: Journal of Parallel and Distributed Computing v 10 n 2 Oct 1990 p 115-129

Publication Year: 1990

CODEN: JPD CER ISSN: 0743-7315

Language: English

Document Type: JA; (Journal Article) Treatment: T; (Theoretical); A; (Applications)

Journal Announcement: 9103

Abstract: Two hardware mechanisms are mainly used for data sharing among processing elements in multiprocessors: message passing in loosely coupled multiprocessors and shared memory in tightly coupled multiprocessors. The former has communication overhead and the latter has shared memory contention. Moreover, in **image** processing, inefficient data input and output schemes are also limitations on performance. In this paper, Flexibly (Tightly/Loosely) Coupled Multiprocessors (FCM) for **image** processing are proposed in order to alleviate these disadvantages. A variable space memory scheme, in which a set of adjacent memory modules can be merged by a dynamically **partitionable bus**, is proposed to realize FCM. These architectures are quantitatively analyzed and simulated on the iPSC/1 (Intel's Personal SuperComputer), a hypercube multiprocessor. Parallel algorithms for region labeling and median filtering are simulated on the proposed architectures. The performance of FCM shows remarkable improvement over that of iPSC/1. (Author abstract) 21 Refs.

Descriptors: COMPUTER SYSTEMS, DIGITAL--*Multiprocessing; **IMAGE PROCESSING**--Equipment; COMPUTER ARCHITECTURE; COMPUTERS, SUPERCOMPUTER

Identifiers: FLEXIBLY COUPLED MULTIPROCESSORS; LOOSELY COUPLED MULTIPROCESSORS

Classification Codes:

722 (Computer Hardware); 723 (Computer Software); 741 (Optics & Optical Devices)

72 (COMPUTERS & DATA PROCESSING); 74 (OPTICAL TECHNOLOGY)

13/5/7 (Item 7 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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02919836 E.I. Monthly No: EIM9006-026304

Title: Scheduling and binding algorithms for high-level synthesis.

Author: Paulin, Pierre G.; Knight, John P.

Corporate Source: BNR, Ottawa, Ont, Can

Conference Title: 26th ACM/IEEE Design Automation Conference

Conference Location: Las Vegas, NV, USA Conference Date: 19890625

E.I. Conference No.: 13186

Source: Proceedings - Design Automation Conference. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 89CH2734-2), Piscataway, NJ, USA. p 1-6

Publication Year: 1989

CODEN: PDAWDJ ISSN: 0146-7123

Language: English

Document Type: PA; (Conference Paper) Treatment: T; (Theoretical); A; (Applications)

Journal Announcement: 9006

Abstract: New algorithms for high-level synthesis are presented. The first performs scheduling under hardware resource constraints and improves on commonly used list scheduling techniques by making use of a global priority function. A design-space exploration technique which combines this algorithm with an existing one based on time constraints is also presented. A second algorithm is used for register and bus allocation to satisfy two criteria: the minimization of interconnect costs and the final register (bus) cost. A clique **partitioning** approach is used where the clique graph is pruned using interconnect affinities between register (bus) pairs. Examples from the literature were chosen to illustrate the algorithms and to compare them with four existing systems. 27 Refs.

Descriptors: COMPUTER PROGRAMMING--*Algorithms; COMPUTER **GRAPHICS**

Identifiers: LIST SCHEDULING; GLOBAL PRIORITY FUNCTION; BINDING ALGORITHMS; **BUS** ALLOCATION; CLIQUE GRAPH; CLIQUE **PARTITIONING**

Classification Codes:

723 (Computer Software); 722 (Computer Hardware)

72 (COMPUTERS & DATA PROCESSING)

13/5/8 (Item 8 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

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02820152 E.I. Monthly No: EIM8911-040150

Title: **IEEE P1596, a scalable coherent interface for gigabyte/sec multiprocessor applications.**

Author: Gustavson, David B.

Corporate Source: Stanford Univ, Stanford, CA, USA

Conference Title: 1988 Nuclear Science Symposium

Conference Location: Orlando, FL, USA Conference Date: 19881109

Sponsor: IEEE, New York, NY, USA; IEEE, Nuclear and Plasma Sciences Soc, New York, NY, USA; Lawrence Berkeley Lab, Berkeley, CA, USA; Lawrence Livermore Natl Lab, Livermore, CA, USA; Stanford Linear Accelerator Cent, Stanford, CA, USA; et al

E.I. Conference No.: 12335

Source: IEEE Transactions on Nuclear Science v 36 n 1 pt 1 Feb 1989. p 811-812

Publication Year: 1989

CODEN: IETNAE ISSN: 0018-9499

Language: English

Document Type: JA; (Journal Article) Treatment: X; (Experimental)

Journal Announcement: 8911

Abstract: IEEE P1596, the Scalable Coherent Interface (SCI), formerly known as SuperBus, is based on experience gained during the development of FASTBUS (IEEE 960), Futurebus (IEEE 896.1) and other modern 32-bit buses. SCI goals include a minimum bandwidth of 1 Gb/s per processor; efficient support of a coherent distributed-cache **image** of shared memory; and support for segmentation, bus repeaters, and general switched interconnections like Banyan, Omega, or full crossbar networks. To achieve these goals, SCI must sacrifice the immediate handshake characteristic of the present generation of **buses** in favor of a packetlike **split**-cycle protocol. Wire-ORs, broadcasts, and even ordinary passive bus structures must be avoided. However, a lower performance (1 Gb/s per backplane instead of per processor) implementation using a register insertion ring architecture on a passive backplane appears to be possible using the same interface as for the more costly switch networks. The author summarizes current directions and reports the status of the work in progress.

Descriptors: *COMPUTER INTERFACES; DATA PROCESSING--Data Transfer;

COMPUTER SYSTEMS, DIGITAL--Multiprocessing

Identifiers: FASTBUS (IEEE 960); SCALABLE COHERENT INTERFACES; SWITCHED INTERCONNECTIONS

Classification Codes:

723 (Computer Software); 722 (Computer Hardware)

72 (COMPUTERS & DATA PROCESSING)

13/5/9 (Item 9 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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02656064 E.I. Monthly No: EI8810096614

Title: CLIP7A IMAGE PROCESSOR.

Author: Fountain, Terry J.; Matthews, K. N.; Duff, Michael J. B.

Corporate Source: Univ Coll London, Engl

Source: IEEE Transactions on Pattern Analysis and Machine Intelligence v 10 n 3 May 1988 p 310-319

Publication Year: 1988

CODEN: ITPIDJ ISSN: 0162-8828

Language: English

Document Type: JA; (Journal Article) Treatment: A; (Applications)

Journal Announcement: 8810

Abstract: A description is given of the CLIP7 **image** -processing chip. The device is implemented as a custom designed integrated circuit and contains a single processing element for use in arrays of processors. The chip uses 16-bit internal and 8-bit external data **buses** and **divides** crudely into two major sections: data processing and data input/output. The first structure to be assembled using these processors is a 256-element linear array, each element incorporating two of the CLIP7 processors. This system, known as CLIP7A, is used both to study the application of partial local autonomy techniques to **image** processing and also as a fast and convenient system for the emulation of other architectures. CLIP7A software and hardware are also described. 28 refs.

Descriptors: **IMAGE** PROCESSING; INTEGRATED CIRCUITS--Applications

Identifiers: CLIP7 CHIP; **IMAGE** PROCESSING CHIP; CUSTOM DESIGNED IC

Classification Codes:

741 (Optics & Optical Devices); 723 (Computer Software); 713 (Electronic Circuits); 714 (Electronic Components)

74 (OPTICAL TECHNOLOGY); 72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

13/5/12 (Item 12 from file: 8)

DIALOG(R)File 8: Ei Compendex(R)

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01196456 E.I. Monthly No: EI8211102966 E.I. Yearly No: EI82103338

Title: VERY SHORT CYCLE LOSS MEASUREMENT BY MICROCOMPUTER.

Author: Augueres, J. L.; Kircher, F.; Sellier, J. C.

Corporate Source: Cent d'Etud Nucl de Saclay, Gif-sur-Yvette, Fr

Source: IEEE Transactions on Magnetics v MAG-17 n 5 Sep 1981, Int Conf on Magn Technol, 7th, MT-7, Karlsruhe, Ger, Mar 30-Apr 3 1981 p 2133-2136

Publication Year: 1981

CODEN: IEMGAQ ISSN: 0018-9464

Language: ENGLISH

Journal Announcement: 8211

Abstract: The improvement of loss theory in superconducting magnets requires measurements during very short cycles. Immediate computation and storage of results and **graphic** display possibilities are needed. A high rate multichannel acquisition system has been developed for this purpose, built-in to a low cost microcomputer based on the S. 100 **bus**. The multichannel acquisition system is **divided** into two boards: an analog board which contains one to four fast A D C (one per channel) and a digital board, containing the memory which is directly accessible through the processor. It is fully programmable: one to four channels, 8 K bytes in selected configuration, logging speed up to 4 MU sec and measurement number. Losses during a 1 msec cycle can be measured with good accuracy.

Because of its flexibility, this system can be used to study other transient phenomena such as quenches or stability measurements. 2 refs.

Descriptors: *SUPERCONDUCTING MAGNETS--*Measurements; MAGNETIC MEASUREMENTS

Classification Codes:

704 (Electric Components & Equipment); 942 (Electrical & Electronic Measuring Instruments); 723 (Computer Software); 701 (Electricity & Magnetism)

70 (ELECTRICAL ENGINEERING); 94 (INSTRUMENTS & MEASUREMENT); 72 (COMPUTERS & DATA PROCESSING)

13/5/14 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

6004901 INSPEC Abstract Number: B9810-6140C-120, C9810-1250-099

Title: **Parallel algorithms for multi-indexed recurrence relations with applications to DPCM image compression**

Author(s): Youssef, A.

Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., George Washington Univ., Washington, DC, USA

Conference Title: Proceedings DCC '98 Data Compression Conference (Cat. No.98TB100225) p.584

Editor(s): Storer, J.A.; Cohn, M.

Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA

Publication Date: 1998 Country of Publication: USA xvi+589 pp.

ISBN: 0 8186 8406 2 Material Identity Number: XX98-00896

U.S. Copyright Clearance Center Code: 1068-0314/98/\$10.00

Conference Title: Proceedings DCC '98 Data Compression Conference

Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Comput. Commun

Conference Date: 30 March-1 April 1998 Conference Location: Snowbird, UT, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Theoretical (T)

Abstract: Summary form only given. DPCM decoding is essentially the computation of a 2-indexed scalar recurrence relation; the two indices are: the row and column positions of the pixels. Although several logarithmic-time parallel algorithms for solving 1-indexed recurrence relations have been designed, no work has been reported on multi-indexed recurrence relations. Considering the importance of fast DPCM decoding of imagery, parallel algorithms for solving multi-indexed recurrence relations merit serious study. We designed novel parallel algorithms for solving 2-indexed recurrence relations, and identified the parallel architectures best suited for them. We developed three approaches: index sequencing, index decoupling, and dimension shifting. To solve a 2-indexed relation in DPCM decoding of an $n \times n$ image, index sequencing breaks down the relation into a sequence of n 1-indexed scalar recurrence relations that must be solved one after another. Each relation is then solved by a parallel $O(n \log n)$ time algorithm on an n -processor hypercube or **partitionable bus**. Thus, the n equations take $O(n \log n)$ time on n processors. Index decoupling, applicable in a common case of DPCM, breaks the 2-indexed relation into n independent 1-indexed recurrence relations, which are then solved simultaneously in $O(\log n)$ parallel time, using $n/\sup 2/$ processors configured as a hypercube or a mesh of **partitionable buses**. (0 Refs)

Subfile: B C

Descriptors: computational complexity; data compression; decoding; differential pulse code modulation; hypercube networks; **image** coding; parallel algorithms; parallel architectures

Identifiers: multi-indexed recurrence relations; DPCM **image** compression; parallel algorithms; DPCM decoding; scalar recurrence relation; column position; row position; logarithmic-time parallel algorithms; parallel architectures; index sequencing; index decoupling; dimension shifting; hypercube; partitionable

Class Codes: B6140C (Optical information, image and video signal processing); B6120B (Codes); C1250 (Pattern recognition); C4240C (Computational complexity); C4240P (Parallel programming and algorithm theory); C4230M (Multiprocessor interconnection)

13/5/15 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

4922787 INSPEC Abstract Number: B9505-6140C-223, C9505-3320B-001

Title: A parallel architecture for performing real time multi-line optical character recognition

Author(s): Andrews, D.; Brown, R.; Caldwell, C.; Baladge, L.; Faules, D.; Hennessey, A.; Murphy, T.; Parkerson, P.; Tesch, E.; Timmerman, R.

Author Affiliation: Dept. of Electr. Eng., Arkansas Univ., Little Rock, AR, USA

p.533-6

Publisher: IEEE Computer Society Press, Los Alamitos, CA, USA

Publication Date: March 1993 Country of Publication: USA xviii+601

pp.

ISBN: 0 8186 3560 6

U.S. Copyright Clearance Center Code: 0094-2898/93/\$3.00

Conference Title: 1993 (25th) Southeastern Symposium on System Theory

Conference Sponsor: IEEE; Univ. of Alabama, Tuscaloosa

Conference Date: 7-9 March 1993 Conference Location: Tuscaloosa, AL,

USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Practical (P)

Abstract: The design of a multiprocessor parallel architecture for performing real-time multiline optical character recognition (MLOCR) is described. MLOCR is a computationally intensive application involving real-time digitization of **images**, pattern recognition, feature extraction, scaling, rotation and gray-scale thresholding, and character recognition. System organization, control and subsystem partitioning of MLOCR algorithms is discussed. System interprocess communications protocols and control of the multiple asynchronous processors are covered. Functional **partitioning** of algorithms onto each processor, **bus** definitions based on real time data communications bandwidths, and system control requirements are also discussed. (5 Refs)

Subfile: B C

Descriptors: feature extraction; hierarchical systems; **image** scanners; interleaved storage; multiprocessing programs; open systems; optical character recognition; parallel architectures; postal services; programmable controllers; real-time systems; rotation; sorting; transport protocols

Identifiers: algorithm functional partitioning; design; multiprocessor parallel architecture; real-time multiline optical character recognition; pattern recognition; feature extraction; scaling; rotation; gray-scale thresholding; subsystem partitioning; interprocess communications protocols; asynchronous processors; bus definitions; data communications bandwidths; system control requirements

Class Codes: B6140C (Optical information, image and video signal processing); C3320B (Control applications to postal services); C5260B (Computer vision and image processing techniques); C5220P (Parallel architecture); C1250B (Character recognition)

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13/5/16 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

03818348 INSPEC Abstract Number: C91016348

Title: The GDC-3 colour graphics plug-in unit

Author(s): Saenger, P.; Dittmar, K.

Journal: Radio Fernsehen Elektronik vol.39, no.8 p.529-32

Publication Date: 1990 Country of Publication: East Germany

CODEN: RFELB6 ISSN: 0033-7900

Language: German Document Type: Journal Paper (JP)

Treatment: Practical (P); Product Review (R)

Abstract: The authors present a plug-in unit that uses the **graphics** display controller U 82720 D to give 8-16 MHz pixel frequencies at 2-4 MHz clocking, without losing the advantages of **dividing** the 16-bit data **bus** into four separate levels each of 4-bits. They explain the controller's wide display mode, soft scrolling, character generator, colour palette, and programming. They give a block diagram of the GDC-3 and its technical data together with timing diagrams for the more important signals. They also give circuit diagrams for the horizontal soft scrolling logic and the sequencer for the character generator. (4 Refs)

Subfile: C

Descriptors: add-on boards; computer **graphic** equipment; controllers; logic circuits

Identifiers: programming; colour **graphics** plug-in unit; **graphics** display controller; wide display mode; character generator; colour palette; timing diagrams; circuit diagrams; horizontal soft scrolling logic; sequencer

Class Codes: C5540 (Terminals and graphic displays); C3230C (Electronic logic)

13/5/17 (Item 5 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

03768089 INSPEC Abstract Number: C91003129

Title: Flexibly coupled multiprocessors for image processing

Author(s): Myung Hoon Sunwoo; Aggarwal, J.K.

Author Affiliation: Comput. & Vision Res. Center, Texas Univ., Austin, TX, USA

Journal: Journal of Parallel and Distributed Computing vol.10, no.2
p.115-29

Publication Date: Oct. 1990 Country of Publication: USA

CODEN: JPD CER ISSN: 0743-7315

U.S. Copyright Clearance Center Code: 0743-7315/90/\$3.00

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: Two hardware mechanisms are mainly used for data sharing among processing elements in multiprocessors: message passing in loosely coupled multiprocessors and shared memory in tightly coupled multiprocessors. The former has communication overhead and the latter has shared memory contention. Moreover, in **image** processing, inefficient data input and output schemes are also limitations on performance. In the paper, Flexibly (Tightly/Loosely) Coupled Multiprocessors (FCM) for **image** processing are proposed in order to alleviate these disadvantages. A variable space memory scheme, in which a set of adjacent memory modules can be merged by a dynamically **partitionable bus**, is proposed to realize FCM. These architectures are quantitatively analyzed and simulated on the iPSC/1 (Intel's Personal SuperComputer), a hypercube multiprocessor. Parallel algorithms for region labeling and media filtering are simulated on the proposed architectures. The performance of FCM shows remarkable improvement over that of iPSC/1. (21 Refs)

Subfile: C

Descriptors: computerised picture processing; multiprocessing systems; virtual machines

Identifiers: flexibly coupled multiprocessors; **image** processing; data sharing; multiprocessors; message passing; shared memory; variable space memory scheme; architectures; iPSC/1; hypercube multiprocessor

Class Codes: C5220 (Computer architecture); C5260B (Computer vision and picture processing)

13/5/18 (Item 6 from file: 2)

DIALOG(R) File 2:INSPEC

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01895293 INSPEC Abstract Number: C82030493

Title: Minimum component-count microprocessor

Author(s): Cheah, Y.C.

Journal: Wireless World vol.88, no.1557 p.61
Publication Date: June 1982 Country of Publication: UK
CODEN: WIWOAA ISSN: 0043-6062
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)

Abstract: This microprocessor circuit brings the number of components required for certain control applications to a minimum and lends itself particularly to machine-control design. Address bus decoding is **divided** up into two 32K-byte pages and the EPROM is situated at 8000 or at 2K-byte **images** up to F800. The M6802's eight interrupt vector bytes should begin at 87F8 or its respective **images**. Two sets of eight i/o lines, A and B, are provided by the M6821 peripheral interface adapter; A addresses are decoded as 7000 and 7001 and B addresses as 7002 and 7003. Locations 0000 to 007F are used for the M6802's 128-byte RAM. (0 Refs)

Subfile: C

Descriptors: computer architecture

Identifiers: address bus decoding; microprocessor circuit;
machine-control design; EPROM; interrupt vector bytes; M6821 peripheral interface adapter; RAM

Class Codes: C5220 (Computer architecture); C5250 (Microcomputer techniques)

13/5/19 (Item 7 from file: 2)

DIALOG(R) File 2:INSPEC

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01878415 INSPEC Abstract Number: B82034709, C82026781

Title: The Data Path generator

Author(s): Shrobe, H.E.

Conference Title: Digest of Papers Spring COMPCON 82. High Technology in the Information Industry p.340-4

Publisher: IEEE, New York, NY, USA

Publication Date: 1982 Country of Publication: USA xvi+418 pp.

Conference Sponsor: IEEE

Conference Date: 22-25 Feb. 1982 Conference Location: San Francisco, CA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P); Experimental (X)

Abstract: The Data Path generator is an experimental design tool constructed as part of the Scheme-81 project. The program is tailored to construct data paths for machines which directly implement interpreters or similar procedures on a microprocessor chip. The system contains a library of procedurally defined cells, advanced **graphic** design tools which make it possible to design such cells using only a **graphics** editor, and a composition program which places and interconnects the cells in a bit-sliced array. The data path so formed offers a high degree of internal parallelism through the use of a **partitioned bus** architecture in which each register is connected to dedicated logical and arithmetic operators via private signal paths. The user of the composition program typically needs to provide only a brief statement of what registers and operators are desired in the data path. The rest of the work is handled by the composition program. The layout of an extremely large data path such as that of the Scheme-81 microprocessor can be accomplished in approximately 30 minutes elapsed time. (4 Refs)

Subfile: B C

Descriptors: circuit layout CAD; microprogramming

Identifiers: Data Path generator; design tool; Scheme-81 project; data paths; microprocessor chip; **graphic** design; bit-sliced array; parallelism; **partitioned bus** architecture

Class Codes: B1130B (Computer-aided circuit analysis and design); C5220 (Computer architecture); C7410D (Electronic engineering)

13/5/20 (Item 8 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2003 Institution of Electrical Engineers. All rts. reserv.

00132556 INSPEC Abstract Number: B70019366, C70009708

Title: Principal details of design drafting for substations by computer

Author(s): Elkins, W.C.

Author Affiliation: Bonneville Power Admin., Portland, OR, USA

Journal: IEEE Transactions on Power Apparatus and Systems vol.PAS-89,
no.3, pt.1 p.457-63

Publication Date: March 1970 Country of Publication: USA

CODEN: IEPSA9 ISSN: 0018-9510

Language: English Document Type: Journal Paper (JP)

Abstract: The Bonneville Power Administration has been developing a system for producing substation design drawings by using automatic data processing methods. Although the system is not yet 100-percent operational on all phases of substation design, it is operational on 115-kV one-line diagrams, **bus** layouts for 500-kV **breaker** -and-a- half and ring-bus schemes, 115-kV customer's service stations, and some switchboard and relay panels. The basic programming structure has been established, and the system offers a practical and economical method of decreasing the man-hour requirements for substation design, where repetitive-type drawings must be produced for construction purposes. The project has been separated into six basic parts: (1) developing the basic logical structure, (2) reducing the **graphical** components to numerical data, (3) retrieving and assembling the necessary components for a specific drawing, (4) transforming the numerical data back into **graphic** form (plotting), (5) generating a 'bill of material,' (6) writing a 'material summary list.' Ways of applying these parts to design drafting are discussed.

Subfile: B C

Descriptors: computer applications; computer-aided design; design engineering; distribution networks; electrical engineering applications of computers; transformer substations

Class Codes: B8350 (Transformers and reactors); B8375 (Substations); C7410B (Power engineering)

13/5/21 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-Eplus

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02059605 JICST ACCESSION NUMBER: 94A0607351 FILE SEGMENT: JICST-E

A 10bit 20MS/s 3V-Supply CMOS A/D Converter for Integration into System VLSIs.

ITO MASAO (1); MIKI TAKAHIRO (1); HOSOTANI SHIRO (1); KUMAMOTO TOSHIO (1);

OKADA KEISUKE (1); YAMASHITA YUKIHIRO (2); KIJIMA MASAKI (2)

(1) Mitsubishi Denki ShisutemuLSIkaiken; (2) Mitsubishi Denki ULSIkaiken

Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report

(Institute of Electronics, Information and Communication Engineers),

1994, VOL.94,NO.124(ICD94 45-57), PAGE.25-31, FIG.11, TBL.1, REF.4

JOURNAL NUMBER: S0532BBG

UNIVERSAL DECIMAL CLASSIFICATION: 621.37.037.3

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: This paper describes a 10-bit 20-MS/s CMOS A/D converter with 3V power supply developed for being integrated into mixed-signal LSIs. In this A/D converter, a circuit technique named "twin encoders" enhances tolerance to substrate noise, together with differential comparators. The bias circuit using a replica of the amplifier is developed for biasing the differential comparator with 3V power supply. Also a subranging architecture with **divided** analog **bus** structure improves dynamic performance of the ADC under 3V power supply. The A/D converter is fabricated in the 0.8.MU.m CMOS process and operates at 20MS/s with showing immunity from substrate noise. (author abst.)

DESCRIPTORS: **image** processing; resolving power; HF; DC power source; CMOS structure; AD conversion; comparator; differential amplifier; VLSI; semiconductor integrated circuit; analog integrated circuit; digital integrated circuit; HDTV

BROADER DESCRIPTORS: information processing; treatment; performance; frequency(Hz); frequency; electric power source equipment; equipment;

MOS structure; device structure; signal conversion; signal processing;
transformation and conversion; amplifier; LSI; integrated circuit;
micro circuit; special television; television
CLASSIFICATION CODE(S): NC05080M

13/5/22 (Item 1 from file: 483)
DIALOG(R)File 483:Newspaper Abs Daily
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06305593 SUPPLIER NUMBER: 62274017
Friday Review: FIRST STEPS IN SHOW BUSINESS:
Hattenstone, Simon
Guardian, p FRIDAY.2
Oct 6, 2000
ISSN: 0261-3077 NEWSPAPER CODE: MG
DOCUMENT TYPE: Commentary; Newspaper article
LANGUAGE: English RECORD TYPE: ABSTRACT

ABSTRACT: Distant Voices, Still Lives was the second instalment of [Terence Davies]'s Liverpool life. The first, his rarely shown Trilogy, is made up of three short movies and is equally brilliant, equally unbearable. The Trilogy shows the young man trying, and failing, to come to terms with his homosexuality. Again, the **images** glue themselves to mind and soul - the solitary woman on the **bus** who **breaks** down and cries till there's nothing left; the father, played by Wilfrid "Steptoe" Brambell, coughing himself to death in a wordless scene that seems to last for ever. With these films Davies quietly reinvented cinema. The camera barely moved, the actors barely acted - they were more like living photographs than movies. He is asked why he chose [Gillian Anderson]. Davies looks a little sheepish as he embarks on a typical story. "When I cast her I hadn't seen The X Files and still haven't because I don't watch television except for the news and some documentaries. I was looking for faces that looked like the Singer Sargent portraits of the belle epoque , and I said, 'That is a John Singer Sargent face, who is she?'" Davies invited her over for a pot of tea, as he does, and it turned out that the American celebrity knew all about the obscure British film-maker. "Apparently, she was a fan. She told me she had seen The Long Day Closes and had cried at the tracking shot over the carpet." I ask Eric Stoltz, who plays Gillian Anderson's unrequited lover, what Davies is like to work with. "[Terry] is a whirlwind of passion. He's a Tasmanian devil crossed with Doris Day. He gets so passionately involved in everything he does that he becomes a dervish of activity and emotion." He looks over to Davies, who is giving someone a huge hug. "He's quite subdued now, but on set when he is up, there is no greater joy in the world than being around him." And when he's down? "When he is in a dark place the world becomes darker. He's a truly lovely and unique artist. I do worry about him out in the world, though, because he feels things so deeply."

DESCRIPTORS: Personal profiles; Motion picture directors & producers
NAMED PERSONS: Davies, Terence

13/5/24 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
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1876294 NTIS Accession Number: PB95-212023
Basis Image Processor PR5200: Module Common Part. Technical Description
Tvete, K.
Norwegian Defence Research Establishment, Kjeller.
Corp. Source Codes: 020610000
11 Jan 95 154p
Languages: English
Journal Announcement: GRAI9514
Also pub. as Norwegian Defence Research Establishment, Kjeller rept. no. FFI/RAPPORT-94/03532.
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S.

customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A08/MF A02

Country of Publication: Norway

Features which are common for Coprocessor modules are implemented in the hardware design Module Common Part. The Module Common Part can roughly be **divided** into three sections: the **Image Bus** Interface, the Coprocessor Service Bus Interface, and the Board Transputer. The Module Common Part design will be included in a Coprocessor board design.

Descriptors: **Image** processing; *Computer systems hardware; Bus conductors; Transputers; Circuit boards; Computer systems programs

Identifiers: Foreign technology; *Module common part; BASIS **image** processor; NTISTFSEAB

Section Headings: 62F (Computers, Control, and Information Theory--Pattern Recognition and Image Processing); 62A (Computers, Control, and Information Theory--Computer Hardware)

13/5/26 (Item 3 from file: 6)

DIALOG(R)File 6:NTIS

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1100563 NTIS Accession Number: PB84-170067

Highway Geometrics, Interactive Graphics , and Laser Mapping

Link, L. E. ; Krabill, W. B. ; Swift, R. N. ; Henry, H. A. ; Glennon, J. C.

Transportation Research Board, Washington, DC.

Corp. Source Codes: 044780000

Report No.: TRB/TRR-923; ISBN-0-309-03612-7

1983 96p

Languages: English

Journal Announcement: GRAI8411

Library of Congress catalog card no. 84-4734.

Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.

NTIS Prices: PC A05/MF A01

Country of Publication: United States

The 15 papers in this report deal with the following areas: prospectus on airborne laser mapping systems; interactive **graphics** in highway design; prediction of the sensitivity of vehicle dynamics to highway curve geometrics by using computer simulation; rehabilitation of existing freeway-arterial highway interchanges; cost-effectiveness of improvements to stopping-sight-distance safety problems; current state of truck escape-ramp technology; designing highways for buses: the New Jersey experience; guidelines for the design and placement of curb ramps; operational effects of two-way left-turn lanes on two-way, four-lane streets; functional analysis of stopping-sight-distance requirements; accident analyses for highway curves; some partial consequences of reduced traffic lane widths on urban arterials; effectiveness of clear recovery zones; comparing operational effects of continuous two-way left-turn lanes; and accident implications of shoulder width on two-lane roadways.

Descriptors: Highway planning; *Design; Traffic control; **Divided** highways; Ramps; Simulation; **Buses** (Vehicles); Urban areas; Accident prevention

Identifiers: NTISNASTRB

Section Headings: 85H* (Transportation--Road Transportation)

13/5/27 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

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Title: Efficient partitioning and scheduling of computer vision and image processing data on bus networks using divisible load analysis

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Abstract: We investigate the data partitioning, distribution, and
scheduling problem for minimizing the total processing time of computer
vision and **image** processing (CVIP) data on bus networks. Using the
recently evolved divisible load paradigm (DLT) [V. Bharadwaj, D. Chose,
V. Mani, T.G. Robertazzi, Scheduling divisible loads in parallel and
distributed systems, IEEE Computer Society Press, Los Alamos,
California, 1996] for processing loads that are computationally
intensive, we design and analyze a scheduler that optimally partitions
the CVIP data and assigns it to the processors in the network in such a
way that the total processing time is a minimum. In addition to the
transmission delay in the network, we consider all the overhead
components that penalize the time performance in the problem
formulation. With this formulation, we derive closed-form solutions for
the optimal processing time when the CVIP data distribution follows a
fixed sequence. We then derive a necessary and sufficient condition for
the existence of an optimal processing time. We then prove an optimal
sequence theorem that identifies a sequence that gives rise to an
optimal processing time among all possible load distribution sequences,
whenever such a sequence of load distribution exists. The performance
of the strategy proposed is also analyzed with respect to speed-up and
processor utilization or efficiency metrics. Several illustrative
examples are shown for the ease of understanding. (C) 2000 Elsevier
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